Ripple Suppression in Capacitive-Gain Chopper Instrumentation Amplifier Using Amplifier Slicing

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***Abstract*— This paper proposes a power-up calibration scheme to mitigate the offset of a capacitive-gain chopper instrumentation amplifier (CCIA), thus suppressing the offset-induced output ripple. In this design, the first stage of the error amplifier is formed by multiple identical slices. Before normal operation, the offset polarity of each slice is determined by reusing the second stage of the amplifier as a comparator. With such polarity information, slices of the first stage are regrouped to achieve a statistical offset reduction. The proposed amplifier has been fabricated in a standard 0.18 μm CMOS process with an area of 0.57 mm^2, achieving an average peak-to-peak output ripple of 58 mV. The amplifier consumes 1.53 μW with a 1.2 V supply. Compared to the state-of-the-art, the calibration time of the proposed scheme is much shorter (14 clock cycles) and the overhead logic consumes no static power after calibration. In addition, the slicing technique provides an extra degree of freedom to the amplifier for bandwidth and noise scaling.**

***Index Terms*— Capacitive-gain chopper instrumentation amplifier, ripple reduction, CCIA, amplifier slicing, bandwidth and noise scaling.**

I. Introduction

DUE to manufacturing imperfections, intrinsic offset exists in all kinds of amplifiers. It results in a non-zero output when the amplifier input is zero. For better comprehension, the output errors are often referred back to the input as input-referred offset, typically in the order of a few to a few tens of millivolts depending on the transistor sizing and adopted process. With the gain requirement of most precision readout circuits, such an offset must be eliminated, or the output could be saturated merely by this offset [1]. Popular practices to reduce offset include using large devices, performing dedicated layout matching, and conducting post-fabrication trimming [2]. However, these techniques cannot withstand temperature variation and offset drift. Additional testing infrastructure is also required for trimming, which greatly increases the cost.

Several dynamic offset reduction methods were developed for offset reduction. For example, auto-zeroing uses a sample-and-hold structure to sample and subtract the offset with two operation phases [3]. However, because the input is disconnected from the amplifier during the sampling phase, techniques using sample-and-hold are not suitable for preserving a continuous-time signal unless a "ping-pong" structure is employed [4]. Auto-zeroing also suffers from noise folding because noise is stored together with the offset due to sampling. Chopping is another offset reduction method that uses frequency translation [5]. By alternating the positive and negative signals at the chopping frequency, the input is modulated to a higher frequency before amplification. Another chopper is then added to reconstruct the signal. Since the signal continuity is preserved, the characteristic of modulation makes it an attractive approach for continuous-time application. However, additional filtering is needed at the end of the whole circuit.

This paper presents an alternative technique to reduce the intrinsic offset during power-up with the help of amplifier slicing. By dividing the amplifier into smaller identical slices, each slice can function separately. This design uses a standard two-stage amplifier with Miller compensation. The calibration scheme is built on a capacitive-gain chopper instrumentation amplifier (CCIA) as a proof of concept [6]. Because of the device offset, CCIA typically suffers from an offset-induced ripple in its output after chopping. During power-up calibration, the inputs of the first stage of the amplifier are shorted, and the second stage is reused as a comparator to determine the polarities of the first stage outputs. Then, the polarity information is used to regroup the slices of the first stage to achieve a statistical offset reduction. The calibration scheme helps reduce the output ripple by more than 10$\times$ (from an average of 628 mV to 58 mV based on measurement) without any additional feedback loop and consumes no extra power after calibration. The overall system consumes 1.53 μW from a 1.2 V supply. It is worth mentioning that the slicing technique provides a degree of freedom to the amplifier for bandwidth and noise scaling.

This paper is organized as follows. Section II revisits the background of CCIA and summarizes the popular ripple suppression methods. Section III presents the proposed offset reduction scheme using amplifier slicing technique along with a mathematical model to examine the best achievable performance. Section IV describes the overall amplifier design and the operation of the offset reduction scheme. Section V shows the measurement results, followed by a brief conclusion in Section VI.

II. Background

A typical CCIA is shown in Fig. 1, which illustrates its topology as well as the formation of offset-induced output ripple [7]. The CCIA consists of an input chopper CH_{in}, a first

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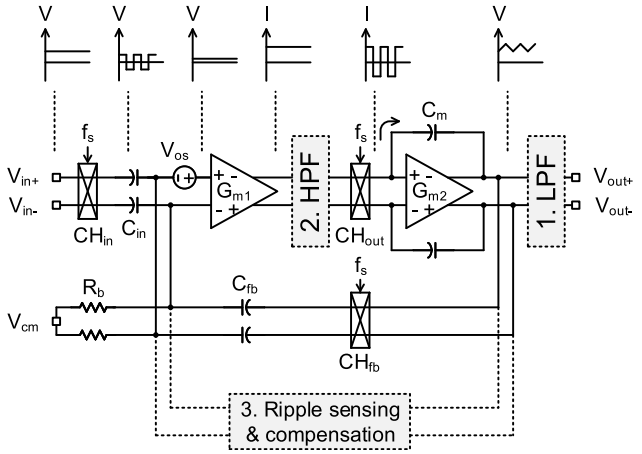

Fig. 1. Existing ripple reduction techniques and formation of offset-induced ripple in a typical capacitive-gain chopper instrumentation amplifier topology (signal not drawn to scale).

stage transconductor g_{m1}, an output chopper CH_{out}, a second stage transconductor g_{m2} and a feedback chopper CH_{fb}. The closed-loop gain is defined by the ratio between the input and the feedback capacitor C_{in}/C_{fb}. During operation, the input signal is firstly modulated by CH_{in} to the odd harmonics of f_s, amplified by g_{m1}, finally demodulated by CH_{out} to DC. The offset V_{os} is amplified and appears as a square wave after the chopper CH_{out}, which is then filtered by a low-pass filter (LPF) formed by g_{m2} and the Miller compensation capacitor C_m. As a result, a triangular ripple (when C_m is sufficiently large), which is proportional to the offset magnitude, appears at the output of g_{m2}, where

$$V_{ripple} = \frac{|V_{os}| \cdot g_{m1}}{2 f_s \cdot C_m}. \tag{1}$$

The accompanied ripple could easily saturate the amplifier output if it is not suppressed [7].

Different ripple suppression techniques were proposed to reduce the output ripple. For example, as shown in Fig. 1, an LPF can be added to perform ripple smoothing [8]. However, implementing an LPF with low cutoff frequency requires a huge chip area, and the input signal, once saturated by the large output ripple, cannot be reconstructed [5].

A better way is to remove the offset-induced voltage/current after the first stage, located between g_{m1} and g_{m2} of Fig. 1. A high-pass filter (HPF) can be added after the first stage to block the offset-induced DC signal, for example by inserting a capacitor between g_{m1} and CH_{out} [9]. However, charges are accumulated on the newly inserted capacitor instead and could saturate the output of g_{m1}. Thus, additional circuits are required to compensate this current. In addition, the input common-mode voltage of g_{m2} should be set separately as all DC components from the first stage are attenuated.

Another way is to add a notch filter between CH_{out} and g_{m2} to remove the ripple by setting orthogonal timing to the chopping and notch filtering signals [10]. A notch filter, which can be implemented by using simple switches and capacitors, is very power- and area-efficient. However, introducing a filter into the signal path directly could decrease the circuit stability and extra effort is needed for frequency compensation [7].

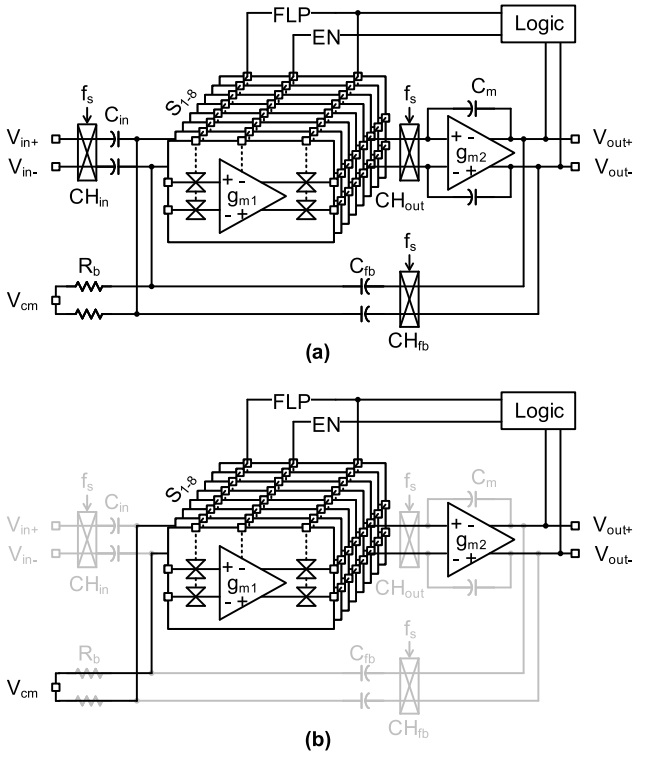

Fig. 2. Schematic of (a) a CCIA with amplifier slicing technique for ripple reduction, and (b) amplifier configuration during ripple reduction.

In addition, an active ripple reduction loop (RRL) is proposed to suppress ripple via feedback instead of using filters [7], [11]. As shown in Fig. 1, RRL performs ripple sensing and adopts an additional feedback loop to null the amplifier offset. However, despite the efficiency of ripple suppression, the RRL must remain active throughout the signal acquisition. Therefore, it inevitably consumes more static power and contributes extra noise. Thus, if offset reduction can be achieved by just reusing the existing structure of CCIA, the expense of additional power can be avoided.

III. Proposed Ripple Reduction Method

The methods mentioned in Section II focus on either using filtering or compensating the offset with a feedback loop. This paper explores another method of ripple suppression by reusing the existing amplifier structure. After a one-time power-up self-calibration, the offset distribution is changed and a smaller initial offset is expected, thus resulting in a smaller output ripple.

A. Amplifier Slicing

A simplified schematic of a CCIA with amplifier slicing is shown in Fig. 2. A single amplifier (the first stage) is split into multiple identical slices and every slice shares the same portion of the original sizing [12]. Since the width of the input pair is reduced, each slice has a smaller transconductance and hence a smaller bandwidth. However, the output impedance r_o of each slice is proportionally larger due to a smaller output biasing current. Thus, the intrinsic gain of all the slices remains unchanged. The amplifier slicing technique allows each slice

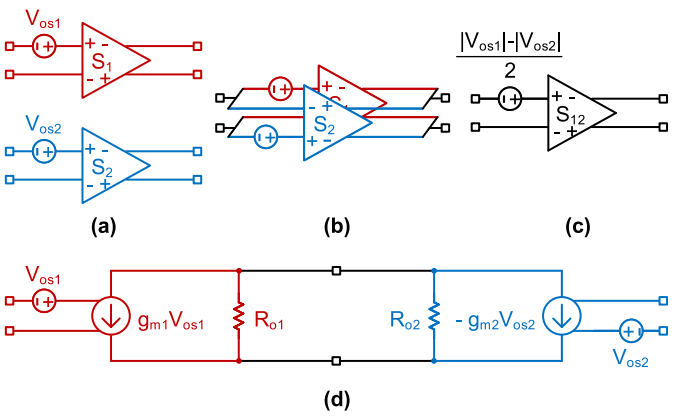

Fig. 3. Demonstration of (a) input-referred offsets of two amplifier slices S_1 and S_2, (b) combining two opposite polarity offsets by flipping one slice (S_2), (c) equivalent input-referred offset of dual slice S_{12} after combining, and (d) small signal model of the dual slice S_{12}.

to work individually. By enabling or disabling some slices, bandwidth and noise scaling can be achieved. When all slices are grouped together, the performance of the newly formed amplifier is almost identical to the original one.

B. Offset Reduction Operation

An offset reduction scheme is proposed based on the amplifier slicing technique and differential-pair matching [13]. As shown in Fig. 3, if two amplifier slices have the same offset polarity, one of the amplifier slices is flipped to make sure the two offsets are opposite to each other. When the two slices are combined, the output offset is obtained from the voltage divider formed by the output impedance of the two slices. The equivalent input-referred offset is then the average of the difference of the two initial offsets. Reusing the structure of a capacitive-gain amplifier, the first stage the amplifier of this design is divided into eight identical slices ($S_{1\text{-}8}$), with each slice sharing one-eighth of the original transistor sizing. Enabling switches are added to enable or disable each slice individually (controlled by EN in Fig. 2). Flipping switches, which change the offset polarity of the corresponding slice, are added to flip the positive and negative inputs and outputs of each slice (controlled by FLP in Fig. 2).

During calibration, as shown in Fig. 2(b), the inputs of the first stage are shorted to the common-mode voltage and C_{m} is disconnected from the second stage, resulting in an open-loop configuration. Any offset appearing in the first stage is amplified by the intrinsic gain $g_{\mathrm{m1}}r_{\mathrm{o1}}$. The second stage acts as a comparator to identify the polarity of the offset for each slice. Since the first stage is divided into eight slices, the calibration consists of three phases. In phase I, $S_{1\text{-}8}$ are enabled one by one consecutively to determine their offset polarities. The control logic then performs corresponding slice flipping. Fig. 4 is an example diagram of a Monte Carlo simulation results for the offset reduction scheme that demonstrate the logic operation. From Fig. 4, slice S_1, $S_{5\text{-}8}$ are flipped after extracting the polarity information in phase I.

In phase II, slices are enabled two by two consecutively, during which the flipping configurations in phase I are retained. The dual slice will flip together whenever any

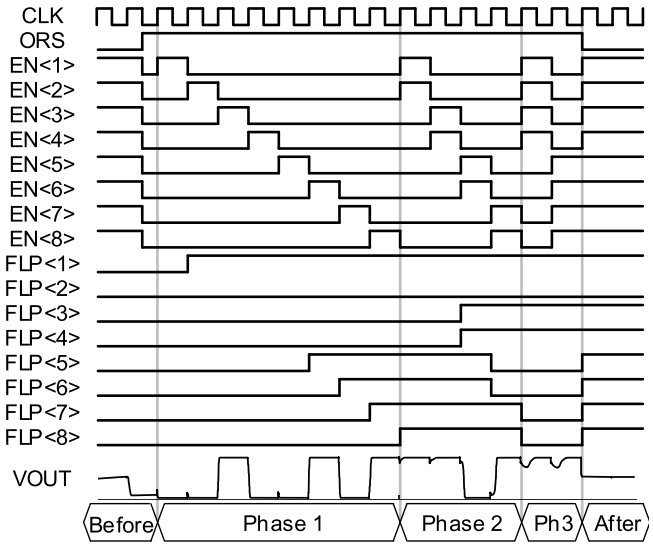

Fig. 4. Example timing diagram of the offset reduction scheme with an offset sequence of (−52, −29, +64, −60, −31, +62, −33, +424) mV from S_1 to S_8.

flipping is needed after comparison. In Fig. 4, dual slice S_{34}, S_{56} and S_{78} are flipped together. In phase III, slices are enabled four by four consecutively along with the previous flipping configurations. Depending on the comparator output, the quad slice will flip together to reverse the offset. Thus, quad slice S_{5678} is flipped then the two quad slices are combined.

Both the differential-pair matching scheme and the proposed slicing scheme use the offset information of the input pairs. However, there are three main differences between the two schemes. First of all, the proposed calibration algorithm statistically reduces the expected offset value via polarity flipping while the matching scheme brute-forces all the combinations and picks the lowest offset. It is true that the proposed algorithm only guarantees a local minimum offset value while the matching scheme secures a global minimum offset value. Thus, a mathematical model is derived in Section III-C to justify the effectiveness of the scheme and the offset distribution of the tested chips is obtained in Section V to show the statistically-reduced offset value. Secondly, the proposed scheme reuses the second stage as the comparator to detect the offset polarity while the matching scheme needs an accurate detector and calibration logic. Since the proposed scheme only needs the offset polarities and they can be extracted with a simple comparator in an open-loop configuration, the second stage can be reused. On the contrary, an accurate detector and calibration logic are needed for the matching scheme to sample the individual offset in a close-loop configuration and reuse the offset value for comparison later on. Last but not least, the total number of comparison cycle for the slicing scheme is $2 \cdot (2^{log_2(N)} - 1) = 2 \cdot (N - 1)$ while the comparison cycle for the matching scheme is C_N^{2N}, where N is the number of slices.

C. Mathematical Modelling

The above scheme relies on a statistical reduction in offset. A mathematical model is developed to estimate the achievable performance of this scheme. According to the central limit

theorem, the amplifier offset V_{os} follows a normal distribution, with

$$V_{os} \sim \mathcal{N}(0,\ \sigma^2), \tag{2}$$

where σ^2 is the variance of the offset. By taking its absolute value (required for ripple estimation), the intrinsic offset $|V_{os}|$ follows a half-normal distribution [14]. The half-normal distribution has a mean of $\sigma\sqrt{2/\pi}$ and a variance of $\sigma^2(1-2/\pi)$, with

$$|V_{os}| \sim \mathcal{H}_{\mathcal{N}}(\sigma\sqrt{\frac{2}{\pi}}, \sigma^2(1-\frac{2}{\pi}))\,. \tag{3}$$

Note that the mean of $|V_{os}|$ is non-zero but depends on the standard deviation σ of the initial offset.

In phase I, the first stage is divided into eight identical slices $S_{1\text{-}8}$, the mean of each of the amplifier offset V_{single} is still zero while its variance is eight times larger. Therefore,

$$V_{single} \sim \mathcal{N}(0,\ 8\sigma^2), \tag{4}$$

and

$$|V_{single}| \sim \mathcal{H}_{\mathcal{N}}(\frac{4\sigma}{\sqrt{\pi}}, 8\sigma^2(1-\frac{2}{\pi}))\,. \tag{5}$$

After performing phase I of the proposed ripple reduction scheme, slices are combined as a dual slice. The offset of dual slice V_{dual} is always the average of the difference between two half-normal distributions, which can be expressed as

$$V_{dual} \sim \mathcal{H}_{\mathcal{N}}(0, 4\sigma^2(1-\frac{2}{\pi}))\,. \tag{6}$$

In phase II, the offset polarity of the dual slice is acquired by shorting the inputs and comparing the outputs. Similarly, the absolute offset magnitude of the dual slice $|V_{dual}|$ is considered. Its mean and variance are derived (see Appendix-A) from the indefinite integral of the probability distribution function of the half-normal distribution. A new distribution named "half-square-normal distribution" is formed and can be expressed as

$$|V_{dual}| \sim \mathcal{H}^2_{\mathcal{N}}(4\sigma\frac{\sqrt{2}-1}{\sqrt{\pi}}, 4\sigma^2(1-\frac{14-8\sqrt{2}}{\pi}))\,. \tag{7}$$

Such a distribution change can be observed in Fig. 5, which is the generated probability density function and cumulative distribution function of offset magnitude. After the regrouping operation of every slice, the distribution becomes more pin-shaped, resulting in a much smaller expected offset value.

After performing phase II, slices are combined as a quad slice. Its offset distribution V_{quad} is simply the average of the difference between two dual slices and follows

$$V_{quad} \sim \mathcal{H}^2_{\mathcal{N}}(0, 2\sigma^2(1-\frac{14-8\sqrt{2}}{\pi}))\,. \tag{8}$$

Using the same iteration process, the offset magnitude of the quad slice $|V_{quad}|$ has a "half-cubic-normal distribution". The offset distribution of the final amplifier V_{final} is the average of the difference between two half-cubic-normal distributions. However, because of the complexity of symbolic derivation [14], numerical simulations are performed to estimate its distribution. The estimated distribution value of $|V_{quad}|$ is

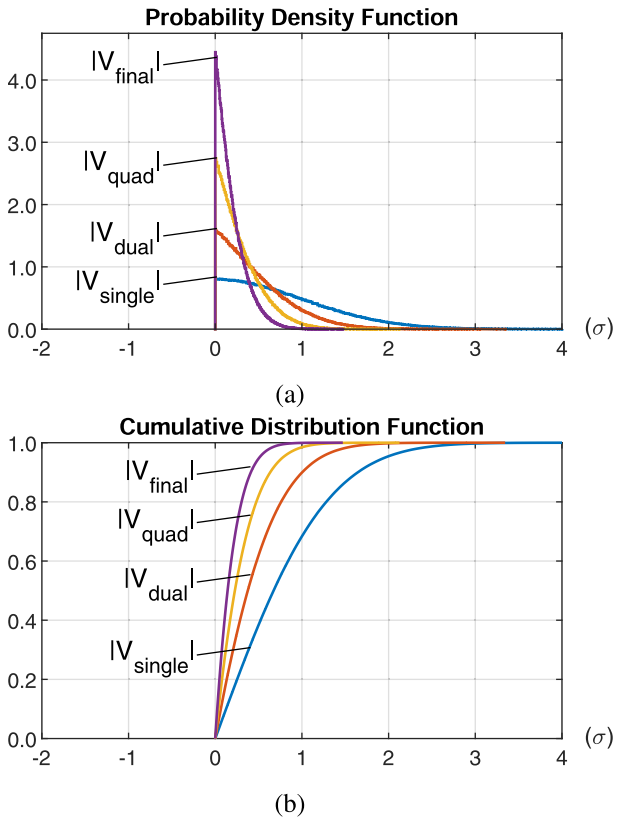

Fig. 5. Generated distribution changes (a) PDF and (b) CDF of offset magnitude during ripple reduction scheme.

($\hat{\mu} = 0.411\sigma, \hat{\sigma}^2 = 0.121\sigma^2$), V_{final} is ($\hat{\mu} = 0, \hat{\sigma}^2 = 0.061\sigma^2$), and $|V_{final}|$ is ($\hat{\mu} = 0.186\sigma, \hat{\sigma}^2 = 0.026\sigma^2$).

To sum up, the expected value (μ) of the offset magnitude changes from $\sigma\sqrt{2/\pi}$ to 0.186σ. In theory, the iteration process can run indefinitely and the variance will keep decreasing until it reaches zero. Nevertheless, this is impractical because infinite slices are required. This can be observed from Fig. 5, in which the distribution curve becomes sharper after every iteration. Note that besides the amplifier offsets, this scheme can also correct other systematic mismatches and yield a better result.

IV. Overall Amplifier Design

The proposed amplifier is designed for near-DC signal amplification. As shown in Fig. 6, it reuses the structure of a standard CCIA with some modifications while maintaining its energy efficiency. The input and feedback capacitors are chosen to be 20 pF and 0.2 pF to set a fixed gain of 100. The unity-gain bandwidth is 200 kHz by choosing the Miller compensation capacitor to be 50 pF. A switched-resistor structure is adopted for input common-mode voltage biasing using a 5 MΩ resistor with a 0.05% duty cycle 5 kHz signal f_{rb} to achieve an equivalent resistance of 10 GΩ [15]. Switched-capacitor common-mode feedback (CMFB) circuits are implemented to stabilize the output common-mode voltage of stage one and two, with non-overlapping control signal Φ_1 and Φ_2. Minimum sized capacitors are used in CMFB to avoid

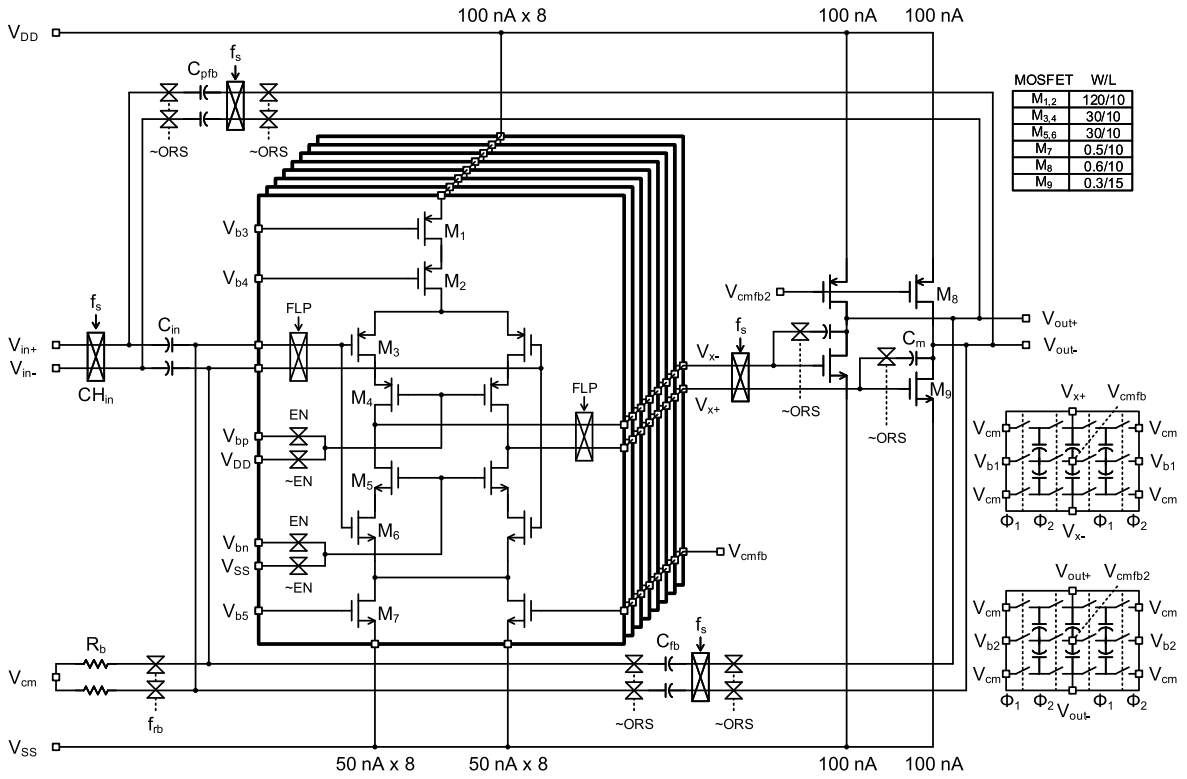

Fig. 6. Schematic of the complete CCIA with amplifier slicing, switches for offset reduction logic, switched-capacitor CMFB and input impedance boosting.

extra loading. The impedance boosting technique with a single chopper and two feedback capacitors is used [7].

A. First Stage

The gain accuracy of the CCIA is directly related to the capacitor ratio and the amplifier open-loop gain. A two-stage amplifier with Miller compensation is implemented to ensure a sufficient open-loop gain ($>$ 120 dB) for decent gain accuracy. The first stage primarily determines the noise floor of the whole system, whereas the second stage determines the output swing and/or driving capability. An inverter-based cascode amplifier is implemented in this design to fulfill the requirement of gain and power efficiency. For energy efficiency design, the inverter-based amplifier outshines other conventional structures because both the PMOS and the NMOS transistors contribute to the transconductance while sharing the same current branch. However, the intrinsic gain of a simple inverter is not sufficient for the proposed design. Thus, a cascode architecture for both PMOS and NMOS is adopted. Each amplifier slice consumes 100 nA ($\times 8$) current with a 1.2 V supply to generate an input transconductance of 2.5 μS ($\times 8$). Note that the shortcoming of the limited input range of inverter-based amplifier is not critical for the CCIA because the input common-mode voltage remains almost constant during operation.

B. Amplifier Slicing

In practice, the first stage g_{m1} is divided into eight identical slices for a number of reasons. First, the number of slices should be a power of two to pair up the slices perfectly. Second, the number of switches is proportional to the number of slices. Logical error may occur during calibration if too many switches are flipping together and the settling time is lengthened. Thus, the number of slices is kept small and minimum size switches are used. Third, large number of switches should be avoid to reduce the switch leakage during normal operation and vary the input common-mode voltage over time.

The input pair work in sub-threshold region to obtain higher current efficiency. In addition to the basic structure, switches are added along with inputs, outputs, and bias. With the enabling and flipping control signals (EN and FLP), the amplifier slice can be enabled or disabled while the inputs and outputs polarity can be reversed.

C. Second Stage

The second stage g_{m2} is a differential class-A common-source amplifier. A 200 nA biasing current is chosen for the second stage to provide an 833 nS transconductance. Two 50 pF Miller compensation capacitors are connected across it to maintain the system stability. For normal operation, the second stage provides the output driving capability and additional open-loop gain on top of the first stage. During calibration, the Miller compensation capacitor, the positive-feedback loop, and the capacitive-feedback loop are disconnected. Thus, the second stage acts as a comparator to distinguish the offset polarity in an open-loop configuration. Since the offset error of the second stage is suppressed by the gain of first stage, the intrinsic offset of the second stage

can be omitted during the comparison. After each comparison, the output of the second stage, which contains the offset polarity information, is latched by the offset reduction logic and used for slice regrouping.

D. Offset Reduction Logic

At power-up, the logic will be triggered immediately to perform offset reduction. A sequential logic is implemented to generate the required control signals for 14 comparison cycles as mentioned in Section III-B. The logic also uses the comparator output to make the slice flipping decisions. The offset of the comparator would not induce significant polarity detection error as it is suppressed by the 80 dB gain of the first stage.

After offset reduction, the logic will enable all slices for normal operation and remain in idle state until the system resets. The signal ORS ("high") is used to indicate the start of the calibration scheme.

E. Other Considerations of This Design

A few non-idealities are considered during the design of this scheme. First of all, switches used for slicing could introduce extra parasitic (e.g., capacitance), which is however not significant for IAs with low operating frequency [5]. Secondly, the second stage g_{m2} also contributes errors to the residual offset. The consequence of second-stage offset is addressed in Section IV-D. Thirdly, assuming the input common-mode voltage is fixed by the voltage bias, the closed-loop gain of the system is set by the capacitor ratio. However, the different current leakage from switches can change the input common-mode voltage over time and induce extra offset. Thus, large OFF-resistance switches are used. Fourthly, the switched-resistor structure is adopted in this design to achieve a common-mode biasing resistor to minimize its noise contribution [15]. Lastly, since the proposed reduction scheme is carried out after system power-on, the temperature-induced offset is taken into account. The proposed scheme can re-run from time to time to calibrate the temperature drift when needed, which is an advantage over other one-time calibration techniques.

V. Measurement Results

The proposed capacitive-gain chopper amplifier with the offset reduction scheme is fabricated in a 0.18 μm standard CMOS process with a 1.2 V supply, consuming 1.53 μW. The power consumption can be further reduced by disabling some slices at the cost of degraded noise performance. Fig. 7 shows the die photo with an active area of 850 μm $\times$ 670 μm. The chopping frequency of the whole system is at 5 kHz, which is slightly lower than the system closed-loop bandwidth at the fixed gain of 100. The achieved CMRR and PSRR at DC are 109 dB and 92 dB, respectively. The worst relative gain accuracy is 0.28% for the measured samples. The histogram of gain variation is shown in Fig. 8.

Fig. 9(a) shows the transient results of eight measured samples during the proposed offset reduction scheme. By shorting the inputs and connecting the outputs to a buffer, output ripples of the samples before and after the scheme are measured. Before reduction, the logic is in idle state and large output ripples can be observed. During the scheme, eight comparisons take place for phase I, four for phase II, and two for phase III. The comparison results can be observed at the output. Towards the end of the 14 cycles, some comparisons require more time to settle. This is because the offset magnitude is getting smaller, which leads to a longer time to establish a large enough output for digital decision. The offset reduction logic is on until it reaches the idle state again. The histogram of output ripple magnitudes is shown in Fig. 9(b). Among the tested samples, the average output ripples before and after the offset reduction scheme are 628 mV and 58 mV, respectively. As mentioned in Section IV-B, the magnitude of ripples can be reduced further with more slices.

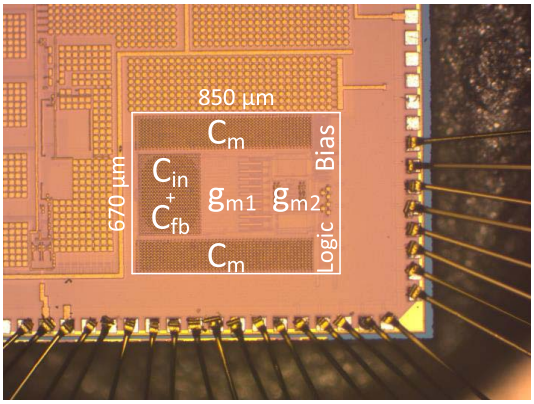

Fig. 7. Die photo of the designed CCIA.

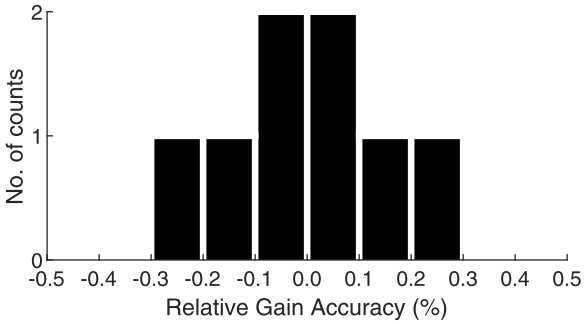

Fig. 8. Histogram of the relative gain accuracy of eight samples.

Fig. 10 shows the transient response of the CCIA to a 10 mV input step signal. The measured output noise spectrum of eight slices enabled versus that of one slice is plotted in Fig. 11. The migration of flicker noise and a corner frequency of 0.25 Hz can be observed. The measured input-referred noise spectrum density (output density divided by signal gain) is 80 $nV/\sqrt{Hz}$. When only one slice is enabled, the input-referred noise degrades to 190 $nV/\sqrt{Hz}$. Meanwhile, the power consumption of the whole system also reduces to around one-eighth. The change in noise spectrum density between enabling eight slices and one slice verifies that the main noise source of this design is from the amplifier slices. By taking current consumption, noise, and bandwidth trade-offs into account, the Noise Efficiency factor (NEF, the lower the better) is used to benchmark our design with other IAs in Table I. Because

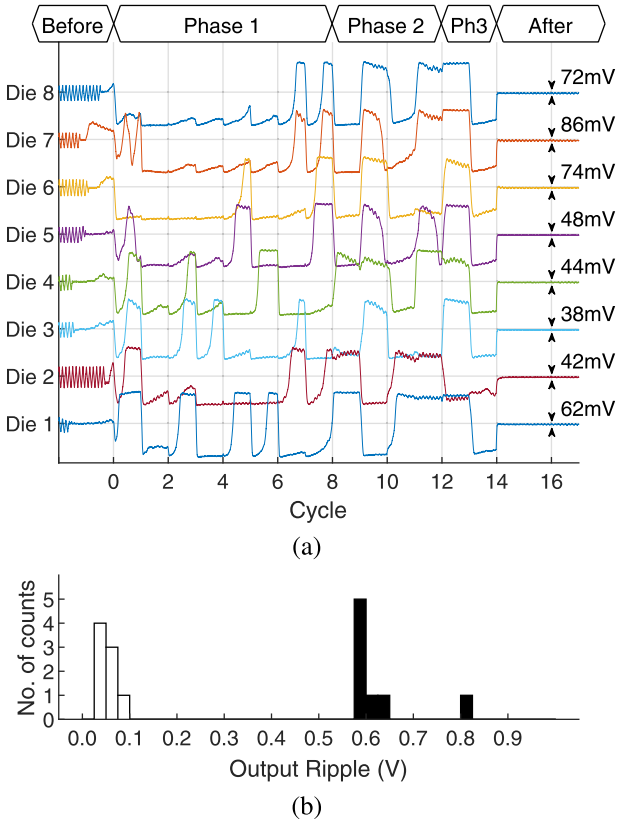

Fig. 9. (a) Measurement results of eight samples during offset reduction and output ripple after reduction, and (b) histogram of the peak-to-peak output ripple voltages before (black) and after (white) the offset reduction scheme.

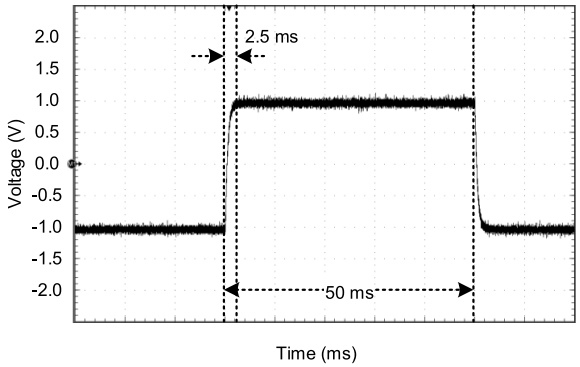

Fig. 10. Step response of the designed CCIA with a 10 mV input at 20 Hz.

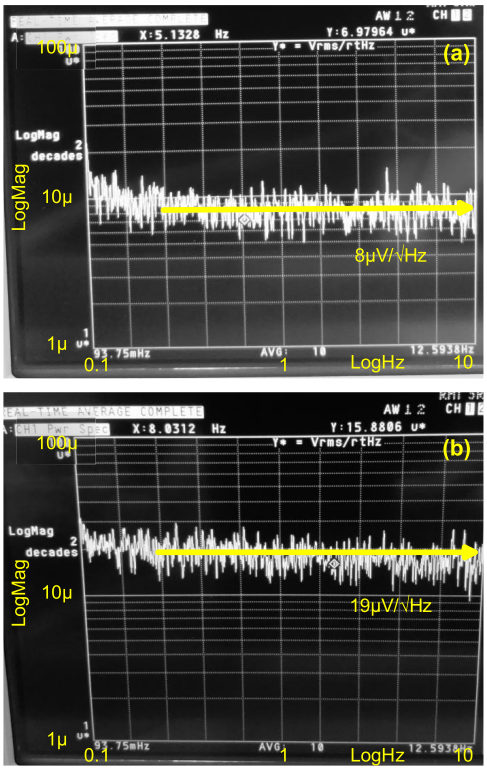

Fig. 11. Measured output noise spectrum with (a) eight slices enabled and (b) one slice enabled in 0.1–10 Hz band.

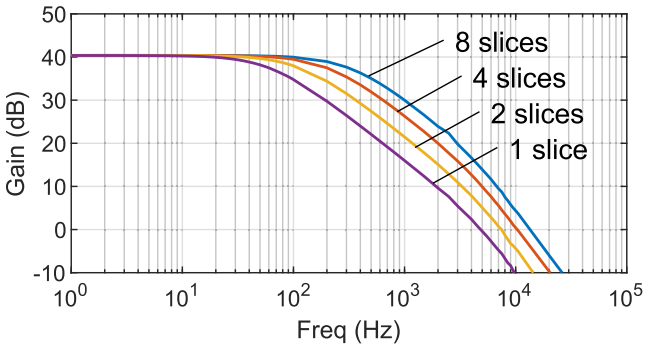

Fig. 12. Testing result of the closed-loop frequency response of different slice configurations with a 4.5 pF loading.

additional active circuity and power consumption for ripple reduction are avoided, the noise efficiency of this design is among the state-of-the-art as indicated by its low NEF.

Bandwidth scaling is another feature of the slicing scheme besides offset reduction. Fig. 12 shows the measured gain and bandwidth of different slice configurations with a loading of 4.5 pF. By disabling some slices, the transconductance of the first stage will be reduced, resulting in a lower bandwidth. For sensor node readout, bandwidth requirement of different sensors often varies. Giving an extra degree of freedom to the amplifier allows users to do a better trade-off between performance and energy efficiency. The offset reduction scheme with fewer slices enabled is not as efficient as the one using all slices. However, since the transconductance is much lower when fewer slices are enabled, the output ripple also reduces proportionally.

Table I summarizes the performance of the proposed CCIA and compares it with other state-of-the-art designs. The competitive result is achieved by inheriting the energy efficiency of a CCIA and reusing its structure for offset reduction. This is reflected by a low NEF of 3.48 and a low Power Efficiency Factor (PEF) of 14.53. Compared to other designs, the residue output ripple of this design is not the minimum, which is reflected in the ripple suppression ratio. However, the major purpose of ripple reduction is to prevent output from saturation and provide enough swing. Post-filtering is no longer necessary in most applications with this level of residue output ripple. When needed, the order of suppression can also be achieved easily with minimal expense of power and area. Benefiting from the slicing technique, part of the slices can be disabled for bandwidth and noise scaling.

TABLE I
COMPARISON OF THE PROPOSED CCIA WITH THE STATE-OF-THE-ART INSTRUMENTATION AMPLIFIERS WITH RIPPLE REDUCTION TECHNIQUES

Design	JSSC 2006 [10]	AD8237 [16]	JSSC 2017 [8]	TCASI 2017 [17]	JSSC 2018 [18]	JSSC 2019 [19]	JSSC 2009 [11]	JSSC 2011 [7]	JSSC 2019 [20]	ISSCC 2013 [13]	**This work**
Technology (CMOS)	600 nm	-	180 nm	320 nm	40 nm	180 nm	700 nm	65 nm	180 nm	180 nm	**180 nm**
Topology	CFIA	CFIA	CCIA	CFIA	CCIA	Chopper	CFIA	CCIA	CCIA	CFIA	**CCIA**
Ripple reduction technique	Notch Filtering	-	LPF	HPF	HPF	HPF	RRL	RRL	RRL	6-Slicing*	**8-Slicing**
VDD (V)	1.8	1.8	0.2, 0.8	3.3	1.2	1.8	5	1	1.8	1.3	**1.2**
Power (μW)	30.6	207	0.79	561	4.5	3.24	1150	1.8	2.16	291	**0.7~1.5**
Chopping frequency (kHz)	125	27	10	20	200	20	40	5	200	500	**5**
Ripple suppression (dB)	54	100	-	~80	-	-	61	63	-	28	**17~26**
Input referred noise (nV/$\sqrt{\text{Hz}}$)	55	68	36	18	85	39	15	60	3.7	13.5	**190~80**
GBW (kHz)	350	200	520	40	40	540	800	700	-	32000	**25.4~203**‡
CMRR (dB)	-	106	85	120	78	100	120	134	134	102	**109**
NEF	8.75	28.1	2.1	10.6	6.35	2.37	8.8	3.3	5.0	7.2	**3.48**
PEF	137.8	1421	1.6	370.8	48.4	10.11	387.2	10.89	45	67.4	**14.53**
Area (mm^2)	0.7	-	1	0.57	0.053	0.2	4.8	0.1	0.73	0.06	**0.57**

*By rearranging the 12 input pairs (6 slices) and brute-forcing the best combination with lowest offset using 924 cycles.
‡System bandwidth is measured with a 4.5 pF loading.

VI. CONCLUSION

A capacitive-gain chopper instrumentation amplifier is implemented in a 0.18 μm standard CMOS process in an area of 0.57 mm^2 with the proposed calibration scheme using the amplifier slicing technique to reduce its intrinsic offset. The first stage of the amplifier is sliced into eight identical slices and the polarity information of each slice is obtained by using the second stage as a comparator. Then, the first stage is regrouped to achieve a statistical offset reduction. A mathematical model is developed to justify the progression of the offset distribution. As there is little extra analog circuitry added to the proposed offset reduction scheme, it has a high energy efficiency. This is also reflected in a low Noise Efficiency Factor, which makes it suitable for universal sensor application. The slicing technique also provides an extra degree of freedom for the amplifier to achieve dynamic bandwidth and noise scaling.

APPENDIX A

The mean and variance of a distribution is derived by evaluating its first raw moment and second central moment. The formulae below show the derivation for half-normal distribution and half-square-normal distribution.

PDF of half-normal distribution:

$$f(x;\sigma) = \frac{\sqrt{2}}{\sigma\sqrt{\pi}}\exp(-\frac{x^2}{2\sigma^2}) \quad \text{for } x > 0 \tag{9}$$

The first raw moment of half-normal distribution:

$$E[X] = \int_0^\infty x f(x) dx \tag{10}$$

$$= \frac{\sqrt{2}}{\sigma\sqrt{\pi}} \int_0^\infty x e^{(-\frac{x^2}{2\sigma^2})} dx \tag{11}$$

$$= \frac{\sqrt{2}}{\sigma\sqrt{\pi}} \int_0^\infty \sigma^2 e^{-y} dy \quad \text{let } y = \frac{x^2}{2\sigma^2} \tag{12}$$

$$= \frac{\sigma\sqrt{2}}{\sqrt{\pi}} \tag{13}$$

The second central moment of half-normal distribution:

$$Var[X] = E[X^2] - E[X]^2 \tag{14}$$

$$= \int_0^\infty x^2 f(x) dx - (\frac{\sigma\sqrt{2}}{\sqrt{\pi}})^2 \tag{15}$$

$$= \frac{\sqrt{2}}{\sigma\sqrt{\pi}} \int_0^\infty x^2 e^{(-\frac{x^2}{2\sigma^2})} dx - \frac{2\sigma^2}{\pi} \tag{16}$$

$$= -\frac{\sigma\sqrt{2}}{\sqrt{\pi}} \int_0^\infty x de^{(-\frac{x^2}{2\sigma^2})} - \frac{2\sigma^2}{\pi} \tag{17}$$

$$= \frac{\sigma\sqrt{2}}{\sqrt{\pi}} \int_0^\infty e^{(-\frac{x^2}{2\sigma^2})} dx - \frac{2\sigma^2}{\pi} \tag{18}$$

$$= \frac{2\sigma^2}{\sqrt{\pi}} \int_0^\infty e^{-y^2} dy - \frac{2\sigma^2}{\pi}, \quad \text{let } y = \frac{x}{\sigma\sqrt{2}} \tag{19}$$

$$= \sigma^2(1 - \frac{2}{\pi}) \tag{20}$$

PDF of the difference of two half-normal distributions:

$$f(z;\sigma) = \int_{-\infty}^\infty f_X(x) f_Y(z+x) dx \quad \text{where } z = x - y \tag{21}$$

$$= \begin{cases} \frac{e^{(-\frac{z^2}{4\sigma^2})}}{\sigma\sqrt{\pi}}(1 + \text{erf}\,\frac{z}{2\sigma}) & \text{for } z \le 0 \\ \frac{e^{(-\frac{z^2}{4\sigma^2})}}{\sigma\sqrt{\pi}}(1 - \text{erf}\,\frac{z}{2\sigma}) & \text{for } z > 0 \end{cases} \tag{22}$$

PDF of half-square-normal distribution:

$$f(z;\sigma) = \frac{2e^{(-\frac{z^2}{4\sigma^2})}}{\sigma\sqrt{\pi}}(1 - \text{erf}\,\frac{z}{2\sigma}) \quad \text{for } z > 0 \tag{23}$$

The first raw moment of half-square-normal distribution:

$$E[Z] = \int_0^\infty z f(z) dz \tag{24}$$

$$= \frac{2}{\sigma\sqrt{\pi}} \int_0^\infty z e^{(-\frac{z^2}{4\sigma^2})} (1 - \text{erf}\, \frac{z}{2\sigma}) dz \tag{25}$$

$$= 2\sigma \frac{2 - \sqrt{2}}{\sqrt{\pi}} \tag{26}$$

The second central moment of half-square-normal distribution:

$$Var[Z] = E[Z^2] - E[Z]^2 \tag{27}$$

$$= \frac{2}{\sigma\sqrt{\pi}} \int_0^\infty z^2 e^{(-\frac{z^2}{4\sigma^2})} (1 - \text{erf}\, \frac{z}{2\sigma}) dz - E[Z]^2 \tag{28}$$

$$= 2\sigma^2 (1 - \frac{2}{\pi}) - \frac{4\sigma^2}{\pi} (2 - \sqrt{2})^2 \tag{29}$$

$$= 2\sigma^2 (1 - \frac{14 - 8\sqrt{2}}{\pi}) \tag{30}$$

APPENDIX B

A summary of the distribution progression during the offset reduction scheme in terms of standard deviation σ is shown below.

$$V_{\text{os}} \sim \mathcal{N}(0,\, \sigma^2) \tag{31}$$

$$|V_{\text{os}}| \sim \mathcal{H}_{\mathcal{N}}(\sigma\sqrt{\frac{2}{\pi}}, \sigma^2(1 - \frac{2}{\pi})) \tag{32}$$

$$V_{\text{single}} \sim \mathcal{N}(0, 8\,\sigma^2) \tag{33}$$

$$|V_{\text{single}}| \sim \mathcal{H}_{\mathcal{N}}(\frac{4\sigma}{\sqrt{\pi}}, 8\sigma^2(1 - \frac{2}{\pi})) \tag{34}$$

$$V_{\text{dual}} \sim \mathcal{H}_{\mathcal{N}}(0, 4\sigma^2(1 - \frac{2}{\pi})) \tag{35}$$

$$|V_{\text{dual}}| \sim \mathcal{H}^2_{\mathcal{N}}(4\sigma \frac{\sqrt{2} - 1}{\sqrt{\pi}}, 4\sigma^2(1 - \frac{14 - 8\sqrt{2}}{\pi})) \tag{36}$$

$$V_{\text{quad}} \sim \mathcal{H}^2_{\mathcal{N}}(0, 2\sigma^2(1 - \frac{14 - 8\sqrt{2}}{\pi})) \tag{37}$$

$$|V_{\text{quad}}| \sim \mathcal{H}^3_{\mathcal{N}}(\hat{\mu} = 0.411\sigma, \hat{\sigma}^2 = 0.121\sigma^2) \tag{38}$$

$$V_{\text{final}} \sim \mathcal{H}^3_{\mathcal{N}}(\hat{\mu} = 0, \hat{\sigma}^2 = 0.061\sigma^2) \tag{39}$$

$$|V_{\text{final}}| \sim \mathcal{H}^4_{\mathcal{N}}(\hat{\mu} = 0.186\sigma, \hat{\sigma}^2 = 0.026\sigma^2) \tag{40}$$

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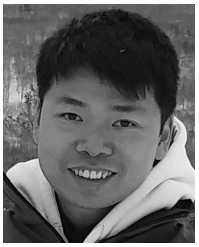

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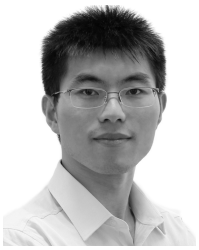

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