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Design and Analysis of A Dual-Band Bistatic Backscatter Circuit for Passive RFID Tags

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***Abstract*—Passive radio-frequency identification (RFID) tags, when placed remotely or in harsh environments, will benefit the most if the communication distance between the tag and reader is vastly improved. The bistatic backscattering technique provides a solution to this problem by separating the carrier and backscattered signal in frequency, which helps mitigate interference. It also decouples the reader from carrier generation by having a separate radio-frequency (RF) emitter and further improves the signal strength by reducing round trip path loss. A dual-band on-chip bistatic backscattering circuit design for passive RFID tags is presented in this paper using a 180 nm CMOS process dissipating 35 μW of power. Post layout simulation results provide a communicable distance of 170 m between the tag and reader at 868 MHz and 60 m at 2.4 GHz when the tag is kept 5 m away from the RF emitter.**

***Index Terms*—Bistatic backscatter, passive RFID, ring oscillator, phase noise.**

I. Introduction

Backscattering technique using various modulation schemes is widely used in low power systems for wireless communication [1]. Unlike systems like WiFi, BLE, etc., the backscatter transmitter just modulates and reflects the received RF signal (carrier) rather than generating a new high-frequency RF signal for power-saving. Many applications such as RFID, low-power sensor networks, and tracking devices are using backscattering to achieve low-cost and power-efficient wireless communication [2].

The backscatter communication system can be classified into two major types: monostatic backscatter system (MBS) and bistatic backscatter system (BBS). Using a passive RFID as an example, an MBS consists of two critical components [3], an RFID tag and a reader, as shown in Fig. 1(a). In MBS, the reader uses the same antenna to emit the carrier and receive the backscattered data from the tag, resulting in signal to noise ratio (SNR) degradation of the received backscatter signal due to interference. Moreover, MBS suffers from a round-trip path-loss. If the tag is placed far from the reader (e.g., 20 m), the modulated backscatter signal strength will be too weak to be decoded (e.g., -92 dBm with 30 dBm reading power). In contrast, for BBS as shown in Fig. 1(b), the reader, an additional RF generator/emitter, and the tag are spatially separated from each other. Thanks to the auxiliary RF emitter, the round-trip path-loss and the doubly-near-far problem in MBS can be mitigated [4]. This extra emitter could be formed by a simple oscillator and a power amplifier, which is more cost-effective than the MBS receiver. A low-cost software-defined radio can then serve as the reader, thus reducing the overall cost of BBS though they are bulkier for deployment [5], [6]. Exhibiting longer transmission distance and lower cost, BBS is highly preferred in future passive RFID design to form wireless sensing nodes.

Using BBS, the communicable tag-reader distance achieved in [7] is 3.4 km using an 868 MHz carrier and 225 m using a 2.4 GHz carrier, consuming 70 μW and 650 μW of power, respectively. The tag and emitter are kept at 1 m apart from each other. However, the communicable distance reduces to 90 m (868 MHz carrier) when the tag-emitter distance is prolonged to 6 m. [8] demonstrated a communicable distance of 268 m using an 868 MHz carrier at an increased packet error rate of almost 10% if the tag-emitter being kept 3 m apart. In [6], the achieved communication distance is 130 m with tag-emitter distance being 2 m. However, these prior designs employ discrete components in their designs and selected high sensitivity reader/receiver (e.g., -110 dBm) with high gain antennas at reader and emitter (e.g., 9 dBi). Particularly, the tag-reader communication distance goes down considerably low when the tag-emitter distance is increased (e.g., to 5$\sim$6 m). To address this issue, we designed a BBS using frequency-shift keying (FSK) modulation for the 2.4 GHz and the 868 MHz band of operation, which provides a predicted reader-tag communication distance of 60 m for 2.4 GHz and 170 m for 868 MHz with only 35 μW power consumption. In this design, a 5 m tag-emitter distance and an 0 dBi tag antenna gain are used for benchmark purposes.

II. Dual-Band Bistatic Backscattering Design

A. BBS Operation

Following the microwave theory, when an antenna interacts with an RF/electromagnetic signal, the antenna will reflect and/or absorb the signal based on its radar cross-section (RCS). For a passive RFID, the antenna is connected directly to the modulator of the tag IC, whose impedance can be controlled digitally to affect the antenna's RCS, allowing the

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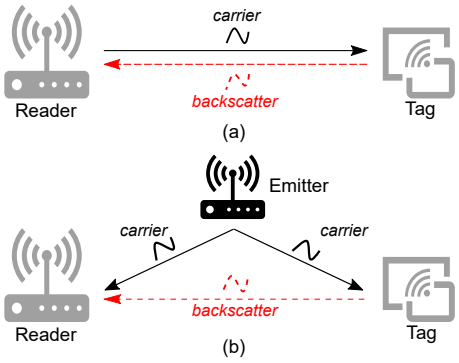

Fig. 1. A simplified (a) monostatic and (b) bistatic backscattering system for passive RFID application.

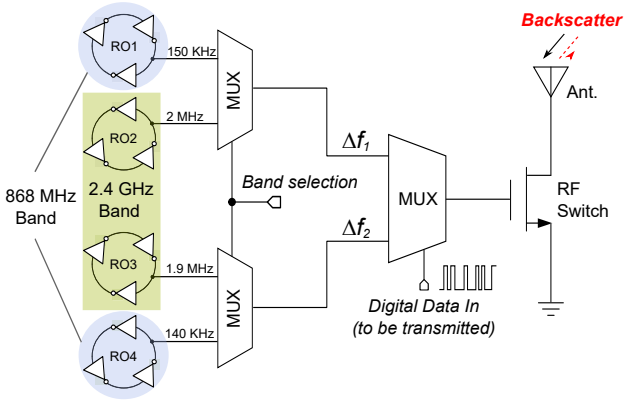

Fig. 2. Block diagram of the dual-band bistatic backscattering circuit, backscatter as mixing process also shown.

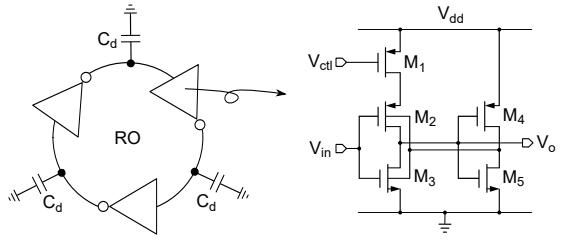

Fig. 3. Typical ring oscillator topology and the low-power delay cell used in the oscillator.

antenna to selectively absorb or reflect the incoming RF signal. This change of operation could introduce a small variation in the reflected signal. For MBS as in Fig. 1(a), the carrier and backscatter signal received by the reader are at the same frequency, and the total power received by the reader is [7]

$$P_{\mathrm{R}}(t) = P_{\mathrm{T}}(t) + \sigma P_{\mathrm{B}}(t) \cdot b(t), \quad (1)$$

where $P_{\mathrm{T}}(t)$ is the signal power transmitted directly from emitter to reader, σ is the tag's RCS, $P_{\mathrm{B}}(t)$ is the backscattered power, and $b(t)$ is the digital bit sequence to be transmitted (0 or 1). In BBS (Fig. 1(b)), the tag modulates the antenna's RCS at a frequency shifted by Δf instead of f_{c} (carrier frequency). Therefore, the frequency component of the received backscatter signal $\sigma P_{\mathrm{B}}(t) \cdot b(t)$ can be decomposed to

$$2sin(f_{\mathrm{c}}t) \cdot sin(\Delta ft) = cos[(f_{\mathrm{c}}+\Delta f)t] - cos[(f_{\mathrm{c}}-\Delta f)t]. \quad (2)$$

It can be seen that the backscattered signal in BBS is present at the positive and negative side of f_{c} with an offset of Δf. Such a displacement helps to mitigate the interference between the carrier and the weak backscatter signal [7].

B. Proposed BBS Design

The block diagram of the bistatic dual-band backscattering circuit designed for passive RFID tag is shown in Fig. 2. The ring oscillators $RO_{1\text{-}4}$ generate the $\Delta f_{1,2}$ signals corresponding to two frequencies of the FSK signal (0 and 1). Based on the carrier frequency, a band selection signal selects the corresponding $\Delta f_{1,2}$ pair. Specifically, for the 2.4 GHz band, the modulation frequency is 2 MHz for data-'1' and 1.9 MHz for data-'0'; for the 868 MHz band, the corresponding frequencies are 150 kHz and 140 kHz. The resulting $\Delta f_{1,2}$ is then modulated by the binary data pattern to be transmitted, which then controls the RF switch and changes the effective RCS of the tag.

Passive RFID tags harvest their energy from the RF transmitted signal and cannot sustain power-hungry circuits. For BBS, RO is the most power-hungry block. To minimize its power draw, inverters with forward body biased transistors are used in the delay cell in our design, which could greatly reduce the transistor's threshold voltage and increase its driving ability [10]–[13]. As shown in Fig. 3, the body terminals of the transistors in the first inverter stage (M_2 and M_3), realized in deep n-well process, are connected to the output of the second inverter (M_4 and M_5). The input voltage V_{in} thus controls the threshold voltages of M_2 and M_3 dynamically. For example, when V_{in} is logic low, the body of M_2 and M_3 are logic low as well, thus M_2 is forward biased while M_3 is zero-biased, and vice versa.

The oscillator in this design is made tunable by controlling the gate voltage of M_1 in order to test the system at different offset frequencies. Considering the frequency drop due to process, corner, and temperature variations, the designed frequency of oscillation is 2.5 MHz and 215 kHz for a nominal control voltage of 0 V under a 1.8 V power supply. Fig. 4(a) shows the oscillation frequency with the change in control voltage, achieving a tuning sensitivity (ratio of change in frequency of oscillation to the change in control voltage) of 1.3 MHz/V. Fig. 4(b) shows the oscillation frequency with power supply changes, providing a sensitivity of 1.6 MHz/V. The oscillators' power consumption is around 35 μW for both bands since their circuit designs remain the same except different delay capacitance C_{d} are used (40 fF for 2.5 MHz and 1.02 pF for 215 kHz).

For an oscillator, both its amplitude and phase could fluctuate due to device noises, while its amplitude fluctuation can be attenuated by the amplitude limiting capability of the ring oscillator. Achieving low phase noise is highly desired as it can

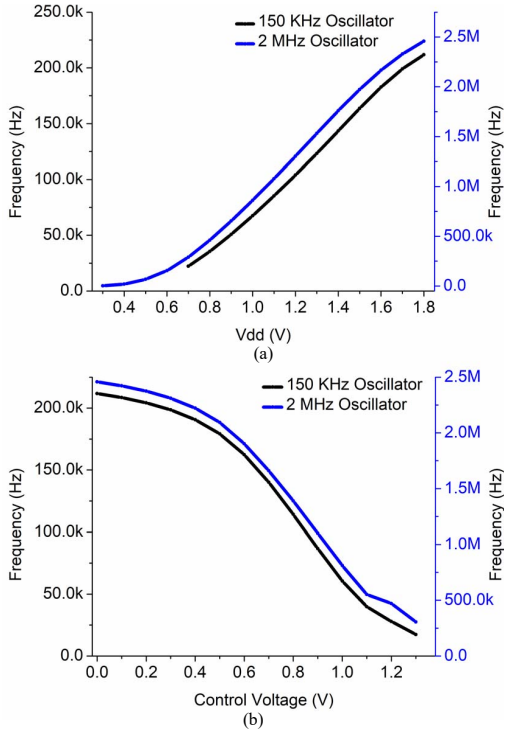

Fig. 4. (a) Frequency vs. power supply, (b) frequency vs. control voltage.

improve the signal to noise ratio of the backscattered signal when mixed with the incoming carrier. The phase noise of the designed ring oscillator can be expressed as [14] [15]

$$L(\Delta\omega) = 10log\left[\frac{(\overline{i_{\rm n}^2}+\overline{i_{\rm p}^2})/\Delta f \cdot \Gamma_{\rm rms}^2}{4q_{\rm max}^2 \cdot \Delta\omega^2}\right] \tag{3}$$

where $\overline{i_{\rm n/p}^2}/\Delta f$, $\Gamma_{\rm rms}^2$, and $q_{\rm max}$ are defined as

$$\frac{\overline{i_{\rm n/p}^2}}{\Delta f} = \frac{8}{3}kT\mu_{\rm n/p}C_{\rm ox}\frac{W_{\rm n/p}}{L}[\frac{V_{\rm dd}}{2} - V_{\rm thn/thp}] \tag{4}$$

$$\Gamma_{\rm rms}^2 = \sqrt{\frac{2\pi^2}{3\eta^3}} \cdot \frac{1}{N^{1.5}} \tag{5}$$

$$q_{\rm max} = C_{\rm d} \cdot V_{\rm swing}. \tag{6}$$

In (3), $(\overline{i_{\rm n}^2}+\overline{i_{\rm p}^2})/\Delta f$ represents the total current noise power from the NMOS and PMOS devices used in the delay cell of the oscillator. In (5), η is 0.75 for a single-ended oscillator and N is the number of stages used in the oscillator. In (6), $C_{\rm d}$ is the equivalent delay capacitance and $V_{\rm swing}$ is the peak-to-peak voltage swing of $C_{\rm d}$.

In this design, to ensure testability of the system for long communication distance between the RFID tag and reader, the reader selected for testing has a sensitivity of -100 dBm. Therefore, the phase noise of the BBS needs to be lesser than this value. For the adopted process, the nominal process parameters are $V_{\rm thn} = 0.45$, $V_{\rm thp} = 0.55$, $C_{\rm ox} = 8.854$ fF/μm^2, $V_{\rm dd} = 1.8$, $\mu_{\rm n} = 670$ cm^2/Vs, and $\mu_{\rm p} = 250$ cm^2/Vs.

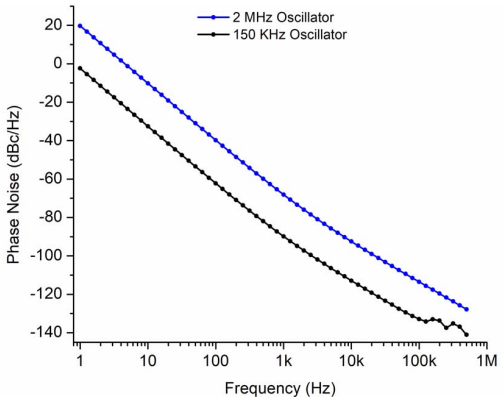

Fig. 5. Phase noise of 2 MHz and 150 kHz oscillator.

The inverters used in the oscillator have the same aspect ratio (0.25/10 μm for NMOS and 0.7/10 μm for PMOS). Therefore, $(\overline{i_{\rm n}^2}/\Delta f)_{\rm n+p} = 1.31 \cdot 10^{-26}$ A^2/Hz, $\Gamma_{\rm rms}^2 = 0.76$, and $q_{\rm max} = 4.8$ fC. With (3), the designed RO phase noise is $L(\Delta\omega) = -138.4$ dBc/Hz, which is slightly higher than the simulated result of -133 dBc/Hz due to process parasitic. Fig. 5 shows the post-layout simulation results of the designed RO's phase noise. The figure of merit [FOM, defined in [16] and copied in (7)] of this design is -169 dBc/Hz by calculation and -163 dBc/Hz from simulation with the value of $p_{\rm avg}$ (power dissipated in mW of the ring oscillator) to be 5.4 μW. Thanks to the dynamic body biasing scheme, this FoM sits at the high-end of typical RO designs, which ranges from -120 dBc/Hz to -170 dBc/Hz for various ROs summarized in [17].

$$\text{FOM} = L(\Delta\omega) - 20\log\left(\frac{f_{\rm osc}}{\Delta f}\right) + 10\log\left(\frac{p_{\rm avg}}{1\text{ mW}}\right) \tag{7}$$

III. Results and Discussion

Post layout simulations were performed on the chip (Fig. 6) whigh occupies 613 $\times$ 392 μm^2 of layout area. Simulated values of S_{11} (return loss) represented in Fig. 7 is obtained, through which the radiated power from the tag is calculated using (8) [7] [18].

$$P_{\rm r} = \left(\frac{P_{\rm t} \cdot G_{\rm t}}{4\pi d_1^2}\right) \cdot K \cdot \left[\frac{\lambda^2 G_{\rm r}}{(4\pi d_2)^2}\right] \tag{8}$$

where $P_{\rm r}$ is the strength of backscattered power from tag, $P_{\rm t}$ is the incident carrier power, K accounts for return loss (S_{11}), $G_{\rm t}$ and $G_{\rm r}$ are the antenna gains of the emitter and the reader respectively. For our system, assuming the power from emitter is 13 dBm with isotropic antenna, antenna gain of the tag is 0 dBi, and the distance between the emitter and tag is 5 meters, the communicable distance achieved between the tag and reader is 170 m for the 868 MHz band of operation and 60 m for the 2.4 GHz band. Communication distance between the tag and the reader is vastly improved in BBS even though it uses an extra RF generator/emitter in comparison to MBS. Table I compares the proposed work with other bistatic backscattering system using FSK modulation.

TABLE I
PERFORMANCE COMPARISON WITH EXISTING BBS DESIGNS.

	6	7	8	This work
Frequency (MHz)	868	2400, 868	868	2400, 868
Tag-Emitter distance (m)	2	1, 1, 6	3	**5, 5**
Tag-Reader distance (m)	130	225, 3400, 90	268	60, 170
BBS power (μW)	n/a	650, 70	n/a	**35**
Transmit power (dBm)	13	30	13	13
Modulation scheme	FSK	FSK	FSK	FSK

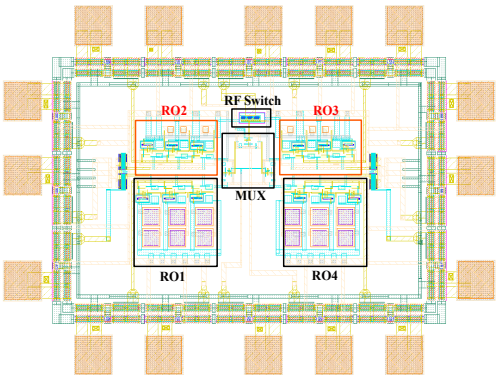

Fig. 6. Layout of the chip

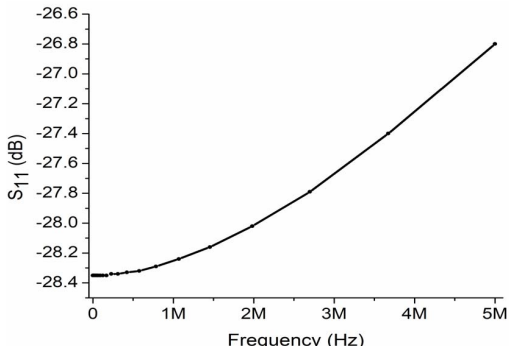

Fig. 7. Return loss in dB across frequency.

The whole tag design consumes around 35 μW of power which is considerably high considering the RFID systems but it is due to the fact that we have made our ring oscillators tunable, to test it under different offset frequencies. Higher power supply is also used in RO design for it to provide enough amplitude to control the RF switch transistor connected to the antenna. The power consumed would drop to a single digit of μ-watts (e.g., to 2$\sim$3 μW, with slight communication distance drop) after removing the frequency tuning function and a lower supply also suffices. As can be seen from Table I, when the distance between tag and the emitter is kept at 5 m, our design achieves nearly double the communication distance between the tag and the reader (at 868 MHz band), while dissipating half the power in comparison to [7], at almost half of the emitted power. With regards to [6] and [8] the communicable distance between the tag and the reader is either improved or are in similar range while maintaining the same emitted power from RF generator/emitter.

IV. CONCLUSION

In this paper, a bistatic backscattering circuit design for passive RFID tags is proposed using FSK modulation. The designed BBS is compact in size and power-efficient utilizing a body-bias controlled delay stage in the oscillator. Simulation results predict that a communicable distance of 170 m between the tag and reader at the 868 MHz band, and 60 m at the 2.4 GHz band, can be attained even if the tag is kept at 5 m away from the emitter while consuming around 35 μW of power. This BBS design is suitable for applications that deploy very dense RFID tags while without deploying readers at the same density.

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