A 32-Step Phase-Compensated Spread-Spectrum RF-PLL With 19.44-dB EMI Reduction and 10-fs Extra RMS Jitter

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***Abstract*— Spread-spectrum clocking (SSC) is an active solution to attenuate electromagnetic interference (EMI) in Gb/s serial communication systems by slightly modulating the phase-locked loop (PLL) output clock frequency. This article presents a phase-compensated spread-spectrum clock generator (SSCG) with the state-of-the-art EMI reduction and clock rms jitter performance. A 32-slice scaled resistor-based buffer is proposed to realize the phase interpolator (PI). The proposed design has no static current and low complexity without active device matching requirement. The 32-slice PI structure can achieve a simulated 22-dB EMI reduction with a 32-step triangular modulation profile. The proposed SSCG chip with a charge-pump-based fractional-*N* radio frequency (RF)-PLL and a source-series-terminated (SST) driver is fabricated using a 55-nm CMOS process. Measurement result shows that EMI reduction of the 5-GHz output clock power spectrum is 19.44 dB under 0.5% down-spread. The rms jitters with SSC-off and SSC-on, adopting a second-order clock recovery in oscilloscope, are 630 and 640 fs, respectively. The normalized power consumption is 9.3 mW/GHz, and the core area occupation is 0.092 mm^2.**

***Index Terms*— Electromagnetic interference (EMI) reduction, phase interpolation, phase-locked loop (PLL), spread spectrum.**

I. Introduction

ELECTROMAGNETIC interference (EMI), caused by coupling or radiation from signals with high frequency and high power, can significantly degrade the performance of electronic circuits. Mostly, in high-speed serial link systems, such as serial AT attachment (SATA), dedicated EMI reduction (typically more than 10 dB [1]) techniques are used to meet the electrical EMI specifications [2]. In the legacy backplane systems, PCI-E, giga-bit-per-second (Gb/s) SerDes links typically have the highest data rate, and they dominate the backplane EMI failures. On the backplane, more than −60-dB crosstalk could be introduced by only one trace (also called an aggressor) on the board, which is even greater than the channel insertion loss in 24-GHz frequency [3]. Techniques, such as ground shielding, can achieve EMI reduction, while at the cost of a bulky design and higher cost. Spread-spectrum clocking (SSC) is an effective method to achieve active EMI reduction without modifying channel structures and has been verified in many high speed SerDes link designs [4], [5]. A spread-spectrum clock generator (SSCG) generates an EMI-reduced high-speed master clock, which is used in the clock and data recovery (CDR) in the receiver (RX) and the serializer in the transmitter (TX), as shown by the SerDes system block diagram in Fig. 1. In our communication system, the SerDes is realized with two 10-Gb/s lanes (2-TX + 2-RX + 1-SSCG). Therefore, it is important to reduce no less than 16-dB EMI to achieve a typical bit-error rate (BER) of 1E-10 [6]. For the adopted half-rate architecture, the SSCG generates a quad-phase clock output clk[3:0], and their frequency is spread at 5 GHz. In the CDR, the quad-phase input clocks are sent to the phase interpolator (PI) to generate recovered clock, whose clock edges are precisely shifted to the center of the input serial data.

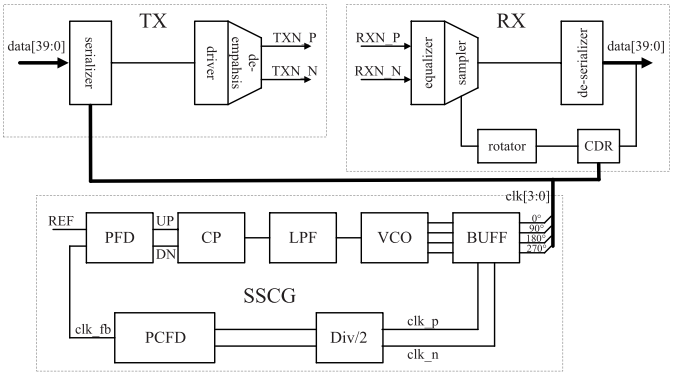

Fig. 1. Block diagram of the SSCG inside a typical high-speed wireline serial communication system.

The operation principle of SSC is to slightly modulate the clock or data link around its center frequency to realize

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power spectrum density (PSD) spreading. There are three typical spread-spectrum clock generator (SSCG) architectures, including input modulation [7], loop filter modulation [8], and fractional division modulation [9], [10]. Input modulation modulates the reference clock to generate a frequency shift in the phase-locked loop (PLL) output [7]. Loop filter modulation modulates the voltage in a passive loop filter, which can be directly transferred to spread-spectrum clock by a voltage-controlled oscillator (VCO) [11]. Fractional division modulation, which modulates the frequency division ratio in the feedback loop of the PLL [13], is a popular SSCG scheme because it is a digital-friendly design and is process scalable.

Two techniques were proposed to realize fractional division modulation for EMI suppression, including $\Sigma\Delta$ modulation and phase compensation [5]. $\Sigma\Delta$ modulation-based fractional frequency divider is a fully digital scheme [14]. However, the use of a feedback frequency dither increases its output jitter [6]. Phase-compensated fractional divider (PCFD), on the other hand, adopts a current-steering DAC to realize the phase interpolation, which penalizes the static system power and exhibits strong process dependence due to the use of active devices in the saturation region [6]. All-digital clock generators using digital delay lines can achieve SSC [15], [16]. However, they have large deterministic jitter and weak EMI reduction performances.

The SSCG topology proposed in this article is based on the classical PCFD with a triangular modulation profile (MP). Instead of using a traditional current-steering DAC, a 32-slice PI with a scaled resistor-based static logic buffer that only occupies an area of 120 μm $\times$ 40 μm is proposed with lower power and larger output swing properties. With an output frequency of 5 GHz and a 0.5% down-spread, a total of 32 modulation steps are achieved to maximize the EMI reduction. The proposed SSCG with a charge-pump-based fractional-N radio frequency (RF) PLL is fabricated in a 55-nm CMOS process. Measurements of the ceramic flip-chip-packaged samples show that the proposed design can achieve the state-of-the-art EMI reduction, as well as jitter performance, among several GHz SSCG designs. With the designed SSC enabled, its introduced extra random jitter and total jitter are only 10 fs and 0.37 ps, respectively.

The remainder of this article is organized as follows. Section II reviews the fundamental theory of the classical fractional-N SSCG architectures. Section III presents the proposed mixed-signal phase compensation scheme for 10-Gb/s SerDes. Section IV describes the charge-pump PLL implementation. Section V reports the measurement results followed by a brief discussion.

II. Classical Fractional-N SSCG Architectures

Spectrum spread can be achieved by modulating the output clock frequency and distributing the narrowband clock energy into a broader band, which reduces the power spectrum densities at the fundamental and odd harmonic frequency tones [17]. Typically, SSC has a small-frequency modulation range, which can be realized by adopting the architecture of a charge-pump-based fractional-N PLL [18], [19]. The output clock

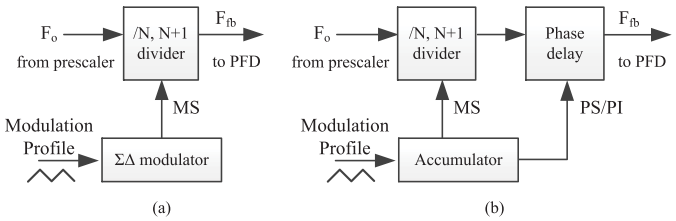

Fig. 2. Block diagram of a fractional-N frequency divider with (a) digital $\Sigma\Delta$ modulation and (b) phase compensation.

frequency can be expressed as

$$F_o = \mathrm{N_{div}} \cdot F_{\mathrm{fb}} \tag{1}$$

where $\mathrm{N_{div}}$ is the fractional-N frequency division ratio. As mentioned, there are two methods to implement the fractional-N frequency divider, including $\Sigma\Delta$ modulation and phase compensation, which are briefed as follows.

The block diagram of a fractional-N frequency divider with a digital $\Sigma\Delta$ modulator is shown in Fig. 2(a), which consists of a $\Sigma\Delta$ modulator and an N/N+1 dual-modulus divider (DMD) [23]. A random modulus selection signal MS is generated by the $\Sigma\Delta$ modulator, which achieves both fractional spur suppression and quantization noise shaping [22]. In this way, the shaped quantization noise is filtered out by the loop LPF. $\Sigma\Delta$ modulator-based fractional-N divider is widely used in RF-PLL systems for its all-digital property. However, in the output frequency of the PLL, in the general purpose, 10-Gb/s SerDes could be configured from sub 1–5 GHz, corresponding to a significant change of the PLL bandwidth according to the actual baud rate. Therefore, the output frequency jitter would be increased because of the mismatch between the dithering and the PLL bandwidth. To address this issue, another approach for fractional-N frequency division is to use phase compensation, as shown in Fig. 2(b) [6]. Instead of an average fractional frequency divider due to modulation dithering, phase compensation technique realizes a truly stable fractional multiple of the oscillator period. Theoretically, the output of the phase-compensated SSCG has lower jitter content, while at the cost of higher power consumption because of the phase interpolation [21].

III. Proposed Phase Compensation SSCG for High EMI Reduction

A. Proposed Architecture

The block diagram of the proposed SSCG, a fractional-N PLL, is shown in Fig. 3(a). It includes a ring VCO, a second-order passive filter, a phase-frequency detector (PFD), a charge pump, and a PCFD. Fig. 3(b) shows the block diagram of the proposed PCFD circuit to achieve high EMI reduction, which consists of a high-frequency/4 divider, an MP, a decoder, a DMD, a phase selector (PS), and a PI. The /4 divider generates an eight-phase output clock ck_d4[7:0]. The MP generates the 31.5-kHz digital triangular waveform, which includes the 5-bit integer division ratio and the 10-bit fractional residual part. The DMD achieves the N/N+1 dual-modulus division, where the divisor is defined by the 5 MSB of

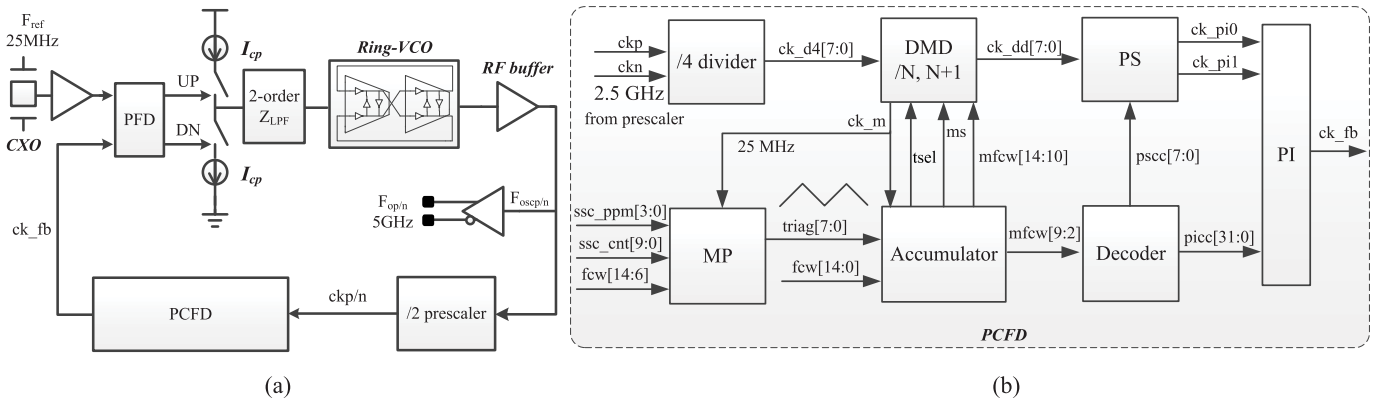

Fig. 3. Block diagram of (a) 5-GHz SSCG and (b) proposed mixed-signal PCFD.

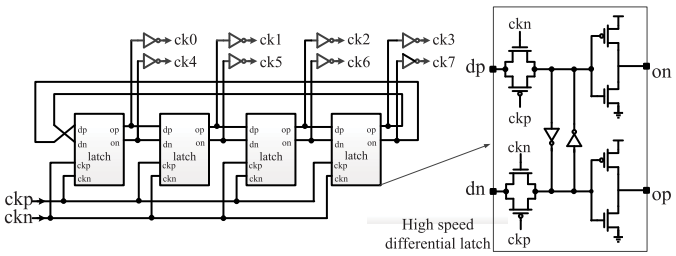

Fig. 4. Block diagram of the eight-phase/4 divider and the schematic of the high-speed differential latch cell.

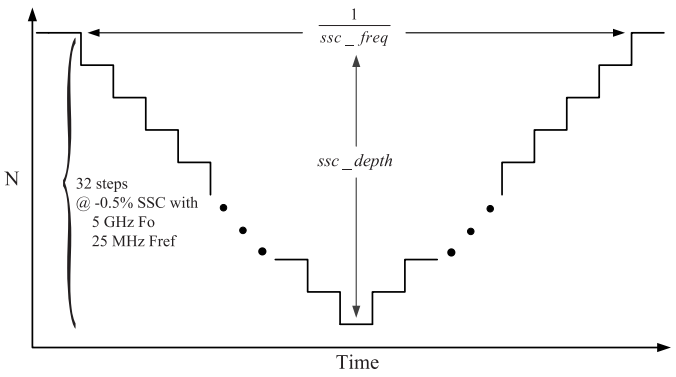

Fig. 5. Triangular MP with modulation depth and modulation frequency definitions.

modulated-frequency control word (mfcw[14:10]), whereas the modulus mode is configured according to the accumulator output ms. The decoder converts the input 8-bit fractional residual mfcw[9:2] into an 8-step PS control word pscc[7:0] and a 32-slice PI control word picc[31:0]. The PS block selects adjacent phase clocks from the eight-phase DMD output controlled by the 3 MSB of the fractional residual. The PI block, realized by the proposed 32-slice scaled-resistor-based buffer, has a 32-step thermometer code resolution controlled by the 5 LSB of the fractional residual.

B. Eight-Phase/4 Divider and SSC MP

Fig. 4 shows the block diagram of the eight-phase/4 divider and the schematic of the high-speed latch. Eight-phase outputs ck[7:0] with 1.6-ns clock periods are generated with a 2.5-GHz input clock ckp and ckn. As shown in Fig. 4, the latch is implemented using differential CMOS static logic with auxiliary inverters to increase its settling speed. In the adopted CMOS 55-nm process, the bandwidth of this latch is up to 8 GHz, which avoids the use of power-hungry current-mode logic (CML) latches as in [24].

In this article, the down-spread spectrum is achieved by superposing a triangular fractional residual on the 15-bit frequency-control word (fcw[14:0]), where fcw[14:10] represents the integer divisor and the fcw[9:0] represents the fractional number. A counter inside the MP is driven by a 25-MHz clock clk_m. ssc_cnt[9:0] is the preset number of counter in the MP, and ssc_cnt_num is the actual value of the present. Once ssc_cnt_num is equal to ssc_cnt[9:0], the counter is switched from the increment mode to the decrement mode, as shown in Fig. 5. The downmodulation depth and modulation frequency are expressed by (2) and (3), respectively. $1/2^{11}$ in (2) is equal to 0.000488218, approximately equal to 500 ppm. ssc_ppm defines the frequency deviation of the SSC, which has a weight of 500 ppm/LSB and ssc_cnt determines the modulation period with a weight of 80 ns/LSB. For the modulation frequency of 31.5 kHz, the ssc_cnt is 397

$$\text{ssc\_depth} = \frac{-\text{ssc\_ppm}}{2^{11}} \tag{2}$$

$$\text{ssc\_freq} = \frac{f_{\text{ck\_}m}}{2 \times \text{ssc\_cnt}}. \tag{3}$$

A 23-bit variable N, representing real-time deviation of frequency as well as the triangular MP of binary form, is calculated in the digital domain according to fcw[14:6], as expressed in the following equation:

$$N = \text{fcw}[14:6] \cdot \frac{\text{ssc\_ppm}}{2^{11}} \cdot \frac{\text{ssc\_cnt\_num}}{\text{ssc\_cnt}} \cdot 2^4 \tag{4}$$

where fcw[14:6] contains 4 bits of fractional number. So, 2^4 must be added to N to convert the fractional part to integer

$$\text{triag} = \frac{\text{fcw}[14:2]}{2^8} - 1 + \frac{\{1, \tilde{}N[22:16]\}}{2^8}. \tag{5}$$

Because of downmodulation, the actual division ratio is equal to the preset division minus deviation. By subtracting

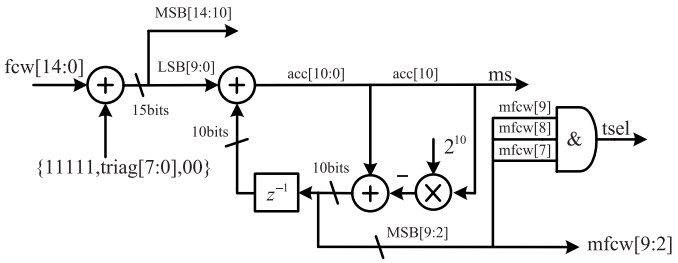

Fig. 6. Block diagram of the accumulator.

TABLE I
TRUTH TABLE OF THE 8-8/32 DECODER

INPUT			OUTPUT							
mfcw[9]	mfcw[8]	mfcw[7]	pscc[7]	pscc[6]	pscc[5]	pscc[4]	pscc[3]	pscc[2]	pscc[1]	pscc[0]
0	0	0	0	0	0	0	0	0	1	1
0	0	1	0	0	0	0	0	1	1	0
0	1	0	0	0	0	0	1	1	0	0
0	1	1	0	0	0	1	1	0	0	0
1	0	0	0	0	1	1	0	0	0	0
1	0	1	0	1	1	0	0	0	0	0
1	1	0	1	1	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	1*

INPUT	OUTPUT									
mfcw[7:2]	picc[31]	picc[30]	picc[29]	picc[28]	picc[27]	.....	picc[3]	picc[2]	picc[1]	picc[0]
0	1	1	1	1	1	.....	1	1	1	1
1	1	1	1	1	1	.....	1	1	1	0
2	1	1	1	1	1	.....	1	1	0	0
.....			.....			.....		.....		
29	1	1	1	0	0	.....	0	0	0	0
30	1	1	0	0	0	.....	0	0	0	0
31	1	0	0	0	0	.....	0	0	0	0
32	0	0	0	0	0	.....	0	0	0	0
33	0	0	0	0	0	.....	0	0	0	1
34	0	0	0	0	0	.....	0	0	1	1
.....			.....			.....		.....		
61	0	0	0	1	1	.....	1	1	1	1
62	0	0	1	1	1	.....	1	1	1	1
63	0	1	1	1	1	.....	1	1	1	1

* ck_dd[0] is delayed by 8/Fosc, when mfcw[9:7] = 111

deviation, which could also express as 1 subtracting bitwise inversion of deviation, from integer divisor, the 8-bit triangular frequency control word triag[7:0] is calculated, as expressed in (5). 2^8 in (5) explained that the N is the decimal division ratio. The number of spread-spectrum steps ssc_step can be calculated by (6). When SSC depth is -0.5% and the integral divisor of fcw[9:0] is 200 for the 5-GHz output frequency and the 25-MHz reference clock, the SSC is 32

$$\text{ssc\_step} = 64(\text{fcw}[14:10] \times |\text{ssc\_depth}|). \tag{6}$$

Fig. 6 demonstrates the structure of the accumulator unit. By subtracting the triangular profile from fcw[14:0] for down-spread, the integral-modulated divisor mfcw[14:10] is generated. The fractional residual passes through an accumulator circuit with MSB detection function. Once the accumulator output acc[10:0] exceeds 2^{10}, the MSB of acc generates a modulus selection pulse signal ms for the following DMD. When mfcw[9:7] is 111, t_sel becomes 0, and the output ck_dd[0] is delayed by $8/F_{osc}$ in the DMD module for phase alignment with ck_dd[7]. Table I shows the truth table of the 8-8/32 decoder. The decoder converts mfcw[9:7] and mfcw[7:2] to its thermometer code, pscc[7:0] and picc[31:0], to control PS and PI, respectively.

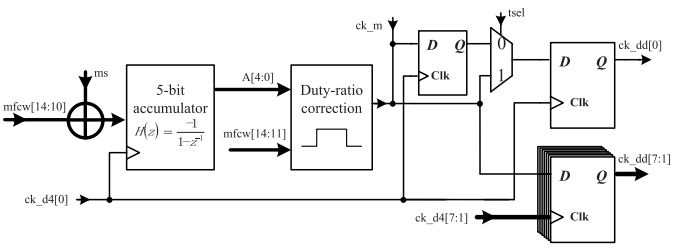

Fig. 7. Block diagram of the N/N+1 DMD module DMD.

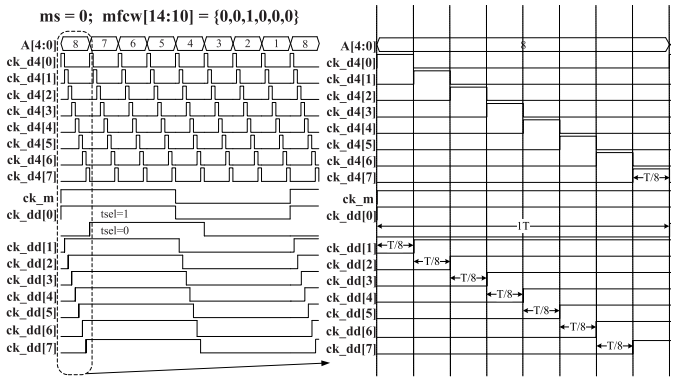

Fig. 8. Timing diagram of the N/N+1 DMD when ms = 0, mfcw[14:10] = 8, and T is 1.6 ns for 5-GHz PLL output ($8/F_{osc}$).

The DMD consists of an accumulator, a duty-ratio controller, a multiplexer, and output registers, as shown in Fig. 7. ck_d4[7:0] is an eight-phase 625-MHz clock bus. The ck_d4[0] with 0 phase delay is used for the programmable clock frequency division, where the divisor is determined by the sum of mfcw[14:10] and ms. To clarify the operation principle of the DMD, its timing diagram is shown in Fig. 8, assuming ms is 0 and mfcw[14:10] is 8. The internal variable A[4:0] gradually decreases and is periodically reset to the divisor. As a result, the /N or /N+1 mode can be interchanged according the value of ms. The digital duty ratio correction is used to ensure the duty ratio R_{duty} of the output clock ck_m (25 MHz in this design) near 50%, as defined in (7). tsel determines whether ck_dd[0] should be delayed by T (1.6 ns for 5-GHz PLL output, $8/F_{osc}$), and sets the phase difference between ck_dd[0] and ck_dd[7] to be $1/F_{osc}$

$$R_{\text{duty}} = \frac{\text{mfcw}[14:10] - \text{mfcw}[14:11] + \text{ms}}{\text{mfcw}[14:10] + \text{ms}}. \tag{7}$$

C. Proposed Phase Compensation Scheme

In the previously reported SSCG design with a state-of-the-art EMI reduction, the PI circuit is implemented by using the current-steering binary-weighted DAC [12], where the linearity depends on the active transistor matching, and it could consume several mA static current for multigigahertz spectrum spread [see Fig. 9(a)]. The phase compensation scheme in this article consists of a phase selection module PS and a phase interpolation module PI [25]. The schematic of the PS with 8-phase-in 2-adjacent phase-out is shown in Fig. 10. The 4:1 multiplexer is implemented using transfer gates. The

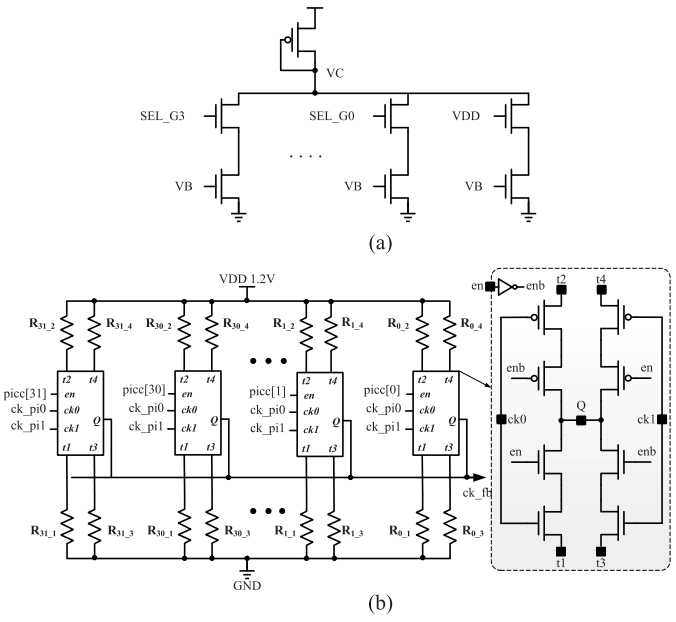

Fig. 9. (a) Schematic of the PI, implemented by using the traditional current-steering binary-weighted DAC [12]. (b) Proposed schematic of the 32-slice scaled resistor-based buffer.

phase difference T_δ of the PS output, ck_pi0, and ck_pi1 is 200 ps. The 32-slice PI module shown in Fig. 9 combines ck_pi0 and ck_pi1 and generates a clock ck_fb that has the same frequency but is phase-interpolated. An *RC* low-pass filter is added in the path of ck_pi in Fig. 9, and the time constant of the filter matches with the frequency of ck_fb to achieve high PI linearity. According to [6], the series resistance R_{lp} and the total load capacitance C_{lp}, including the distributed gate parasitic capacitors of the PI module, should be designed following (9). The phase of the PI output, Φ_{ck_fb}, is determined by enabling the parallel load resistor array according to the thermometer code picc[31:0], and its value is expressed by (11). Comparing with the PI based on a current-steering DAC, the proposed structure shows two advantages. At first, a static bias current is required for the current DAC to keep transistors in the saturation region. On the contrary, the resistor-based buffer in this article is operating at the switching mode (similar to a class-AB inverter amplifier), and as a result, the power consumption of this article becomes smaller. Second, the output voltage swing of a DAC-based PI is smaller than the proposed design, which is limited by operating in the saturation region, but the proposed resistor-based buffer can nearly provide a rail-to-rail output swing.

As shown in Fig. 11, within 45°, a total of 32 steps of phase interpolation can be achieved. To evaluate the linearity of the PI, the mismatch is calculated by comparing the maximum and minimum PI differential nonlinearities (DNLs) as defined by (11). In this article, the simulated PI_{mis} of 52% has no effect on the EMI reduction performance, whereas leads to an increased output clock jitter [6]

$$T_\delta = \Phi_{ck\_pi0} - \Phi_{ck\_pi1} = 200 \text{ ps} \tag{8}$$

$$\tau = R_{lp} \times C_{lp} > 3T_\delta = 600 \text{ ps} \tag{9}$$

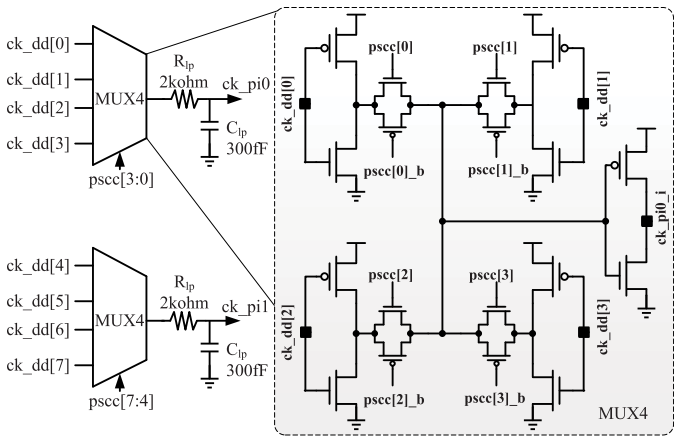

Fig. 10. Schematic of the 8-phase-in 2-adjacent phase-out phase selection module based on 4-to-1 multiplexer.

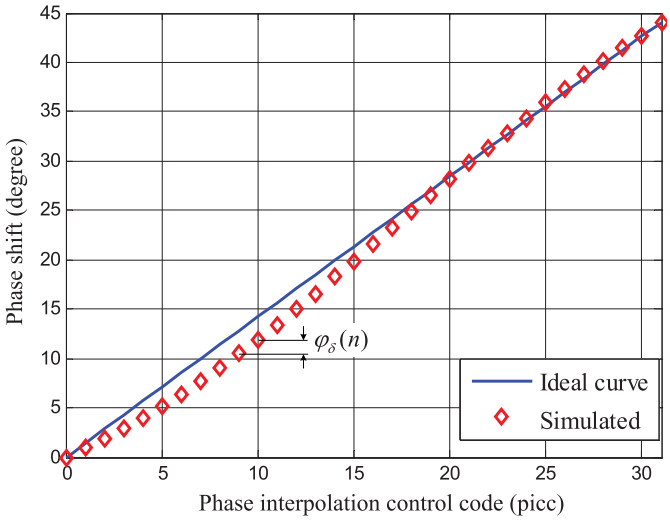

Fig. 11. Simulated phase shift of the proposed 32-slice PI versus picc.

$$\Phi_{ck\_fb} = \alpha \times \Phi_{ck\_pi0} + (1-\alpha)\Phi_{ck\_pi1} \approx \frac{\Phi_{ck\_pi0}}{32}\sum_{n=0}^{31}\text{picc}[n] + \frac{\Phi_{ck\_pi1}}{32}\left(32 - \sum_{n=0}^{31}\text{picc}[n]\right) \tag{10}$$

$$PI_{mis} = \frac{\max(\varphi_\delta) - \min(\varphi_\delta)}{\text{mean}(\varphi_\delta)} = 52\%. \tag{11}$$

D. Charge-Pump PLL and Source-Series-Terminated (SST) Driver Implementation

A classical PFD and charge-pump (CP) scheme is adopted in this PLL [26]. A 40-ps delay is added to the PFD reset path to limit the dead zone of the PFD + CP. With a 25-MHz reference clock and a 5-μA charge-pump bias current, a +/− 0.0015π dead zone can be achieved. A rail-to-rail auxiliary amplifier with a dc gain of 38 dB is used in the charge pump to track the output voltage and attenuate the charge-sharing effect during the switching of up/dn

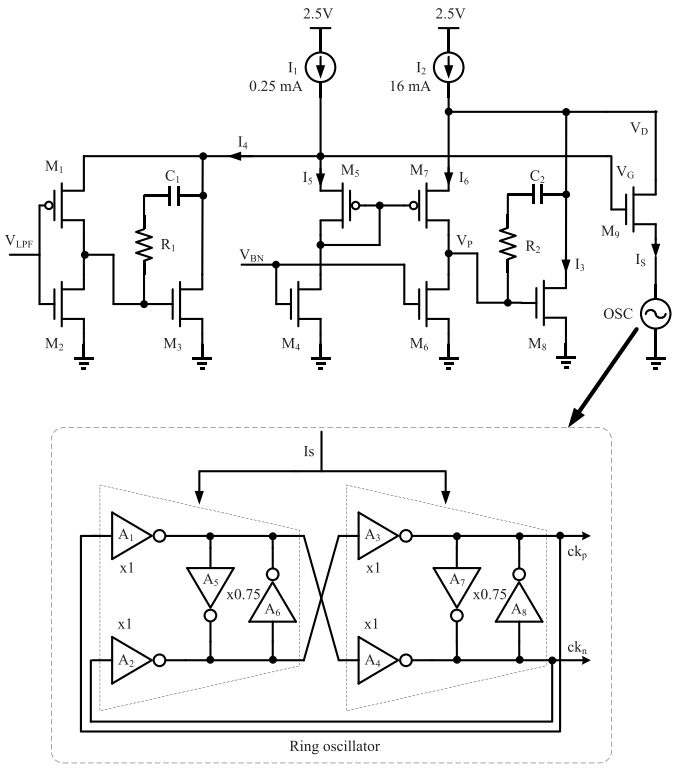

Fig. 12. Schematic of the 5-GHz ring VCO.

and up_n/dn_n. [22]. The schematic of the VCO is shown in Fig. 12. A 2.5-V power supply is adopted to realize wider frequency tuning range and larger output swing. The supply voltage of the ring oscillator (RO) is regulated by the gate voltage of M9, V_G. By assuming that all the transistors are operating in their saturation regions, the relationship between v_{LPF} and v_G can be expressed by the following equation:

$$\begin{aligned} v_G &= \left(\frac{g_{m2}}{g_{m1}} + 1\right) v_{\text{LPF}} \\ &= \left(\sqrt{\frac{\mu_n}{\mu_p}\left(\frac{W}{L}\right)_2 \Big/ \left(\frac{W}{L}\right)_1} + 1\right) v_{\text{LPF}} \\ &\approx 1.27 v_{\text{LPF}} \approx v_D \end{aligned} \tag{12}$$

where g_{m2}/g_{m1} are the transconductance of M2 and M1, respectively, and can be tuned by changing the size of M1 and M2. In this article, the linear range of V_G is 0.9–2.3 V with a 1.27 gain of v_G/v_{LPF}. The RO adopts the inverter-based pseudodifferential topology. Four auxiliary inverter amplifiers with a scaled size of $\times 0.75$ are used to introduce a phase hysteresis [27]. The simulated output frequency range of the oscillator is 1.2–6.9 GHz with 16.3-mA static current drawing from a 2.5-V supply, which corresponds to a large K_{VCO} of 24.5 G. The output buffer of the VCO is ac-coupled inverter amplifiers, as shown in Fig. 13. A 2-kω resistor is used in the feedback path to establish the dc operating point of the buffer. The bandpass transfer characteristic can be described by (13) [27], which is estimated with the peak ac gain that appears at 6.2 GHz

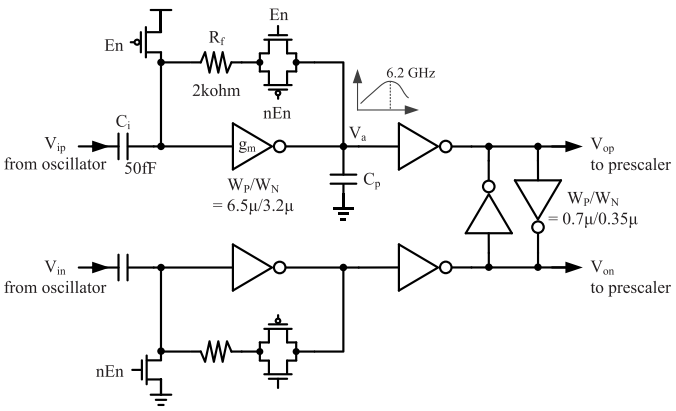

Fig. 13. Schematic of the differential VCO RF buffer.

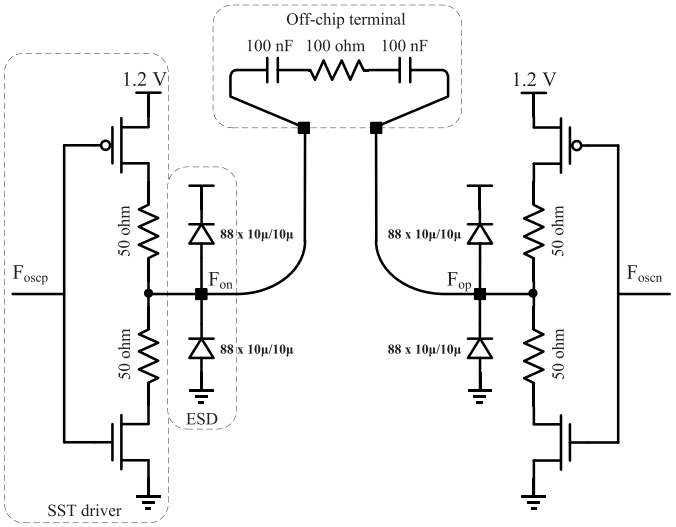

Fig. 14. Schematic of the pseudodifferential SST driver.

$$\frac{V_a}{V_{\text{ip}}} \approx \frac{-s g_m R_f C_i}{g_m + s\left(C_i + C_p + \dfrac{R_i C_f}{r_o}\right) + s^2 R_f C_i C_p}. \tag{13}$$

A pseudodifferential SST driver is implemented in this article for the SerDes TX, as shown in Fig. 14. Compared with the CML driver, the SST circuit offers lower power consumption and wider output voltage swing. ESD diodes are added for the 4-kV human-body-model (HBM) ESD protection. Its output common-mode voltage is 0.6 V and the output is ac coupled through 100-nF capacitors with a 100-ω series terminal resistor. In practice, the SST driver is designed with the multislice topology to achieve terminal resistance configuration and feed-forward equalization [28].

IV. Experimental Results

The proposed SSCG core occupies a chip area of 420 μm $\times$ 220 μm, where the LPF and VCO occupy half of the area and only 120 μm $\times$ 40 μm is consumed by the PI. All the GHz signal lines longer than 50 μm are ground shielded, and all differential lines are equilong and symmetrical. The total

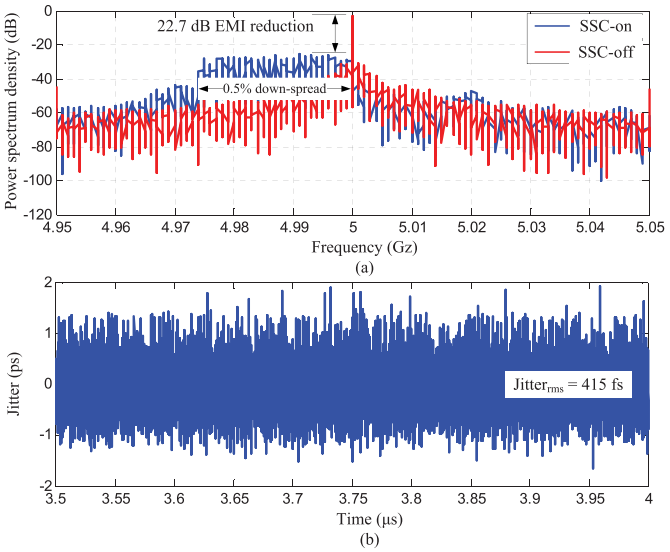

Fig. 15. (a) Post-layout simulated 22.7-dB EMI reduction of the proposed 5-GHz SSCG with/without spectrum spread. (b) Post-layout simulated 415-fs rms random jitter of the proposed 5-GHz SSCG with SSC-off for 2500 clock cycles.

power of the core is 46.54 mW, where about 78% is consumed by the VCO. The EMI reduction function is simulated with the SSC turned on and off. With a 0.5% down-spread at 5-GHz output, the postlayout simulated effective EMI reduction is 22.7 dB, as shown in Fig. 15(a). Random jitter of the 5-GHz output clock is also reported in Fig. 15(b) within 500-ns time span. The postlayout simulated 415-fs random rms jitter is underestimated because the power supply noise is absent in the simulation, which is expected to degrade the SSCG jitter performance by 50%, as shown later in the measurement result. The proposed SSCG chip is fabricated using the 55-nm CMOS process. The chip area, including a SSCG core and two TXs, is about 1 mm^2, whereas the core area of the SSCG is only 0.092 mm^2. Ceramic flip-chip ball grid array (CFCBGA) package is used for high-reliability applications, as shown in Fig. 16(a). The design under test (DUT) is surface-mounted on the ten-layer PCB with Rogers R4350B substrate, as shown in Fig. 16(b). External LDOs provide a 2.5- and 1.2-V power supply. A 25-MHz active crystal oscillator and 200 division ratios were adopted to generate a 5-GHz output frequency with the SST driver. A Xilinx KC705 evaluation board is used to control the test board. The Keysight 33-GHz real-time oscilloscope MSOV334A and a 26.5-GHz signal analyzer N9010A are used to measure the transient and spectrum specifications, respectively. A YIHUA 8508D heater and a CEM portable thermometer are used to measure the chip reliability at different temperatures.

The phase noise of the PLL output from the SST driver with SSC-off is measured at room temperature, as shown in Fig. 17. A −86.01-dBc/Hz phase noise at 1-MHz offset is achieved at the center frequency of 5 GHz. When measuring the phase noise, the spectrum analyzer only supports single-ended RF input. As a result, the common-mode noise and the power supply noise cause phase noise degradation. Meanwhile, because the output is driven by SST, the driver noise is also counted during the phase noise measurement. According to

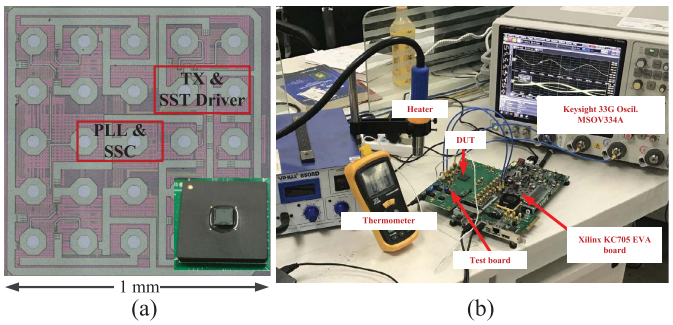

Fig. 16. (a) CMOS 55-nm prototype chip microphotograph of the proposed SSCG with ceramic FCBGA package. (b) Test setup of the proposed design.

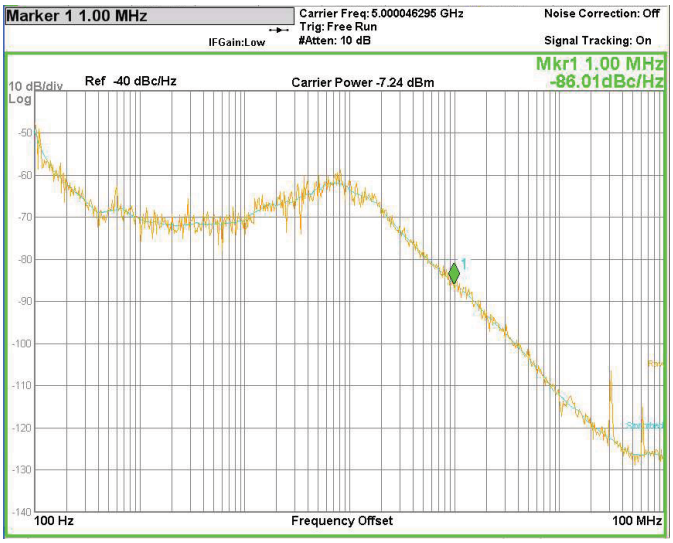

Fig. 17. Measured phase noise of the SST driver differential 5-GHz clock output (SSC-off), −86.01 dBc/Hz at 1 MHz.

the simulation, the pseudodifferential SST driver contributes 1.5-dB phase noise. The simulated differential-output phase noise of the designed 5-GHz VCO core is −94.8 dBc/Hz at the 1-MHz frequency offset, which is about 8 dB better than the measurement result. By integrating the measured phase noise from 100 Hz to 10 MHz, 11.9-ps rms phase jitter is calculated, which is consistent with the 14.9-ps time-domain rms jitter result measured in the oscilloscope by disabling the clock recovery block.

The spectrum spread performance is measured with/without the 0.5% spectrum spreading at room temperature, as shown in Fig. 18. In the measurements, the resolution bandwidth (RBW) and view bandwidth (VBW) are set to 100 and 10 kHz, respectively. The spectrum is averaged in the rms type to avoid transient measurement error. When the SSC function is disabled, the power at the center frequency of 5 GHz is −16.287 dBm. With the SSC enabled, the PSD is down-spread in 25-MHz bandwidth, and the peak PSD is −35.729 dBm, which means a 19.44-dB EMI reduction is achieved with a 0.5% spectrum spreading at 5-GHz output. The measured EMI reduction is about 3 dB lower than the post-layout simulation in Fig. 15, which could be because of the extra power supply noise and transistor mismatch in VCO.

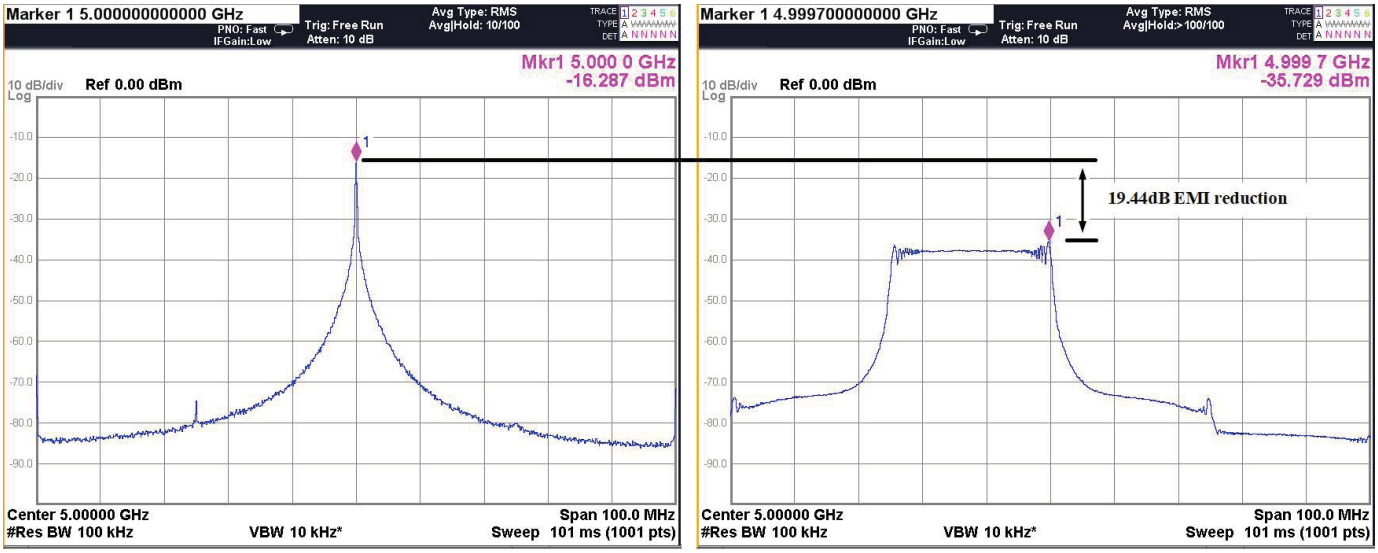

Fig. 18. Measured spectrum density of the SST driver differential 5-GHz clock output, under 100-kHz RBW, with SSC-off (left) and with −0.5% SSC-on (right), proving 19.44-dB EMI reduction.

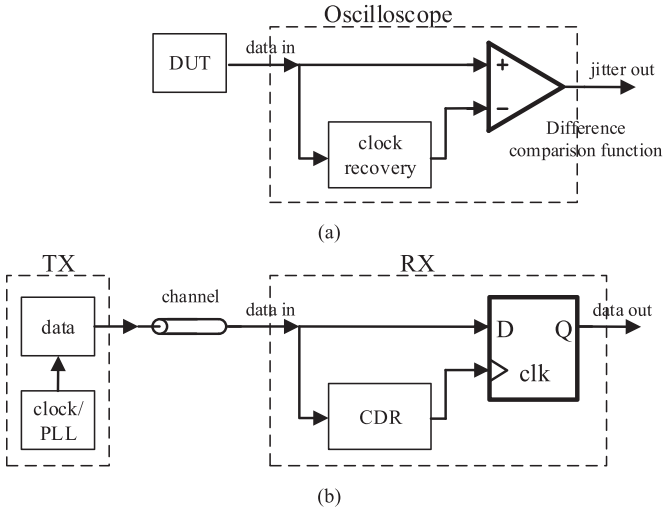

Fig. 19. Jitter measurement diagrams of (a) oscilloscope and (b) serial-link system.

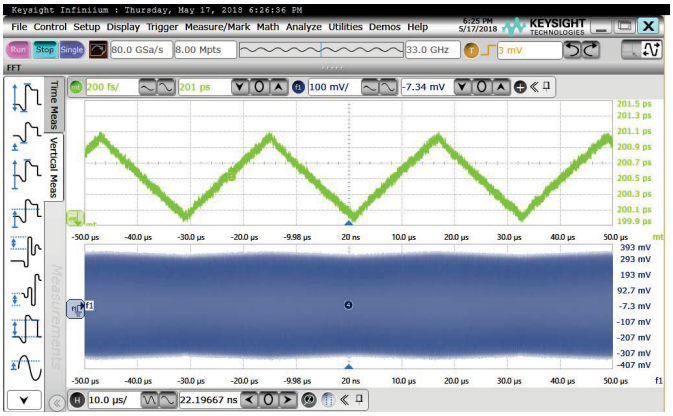

Fig. 20. Measured period of the SST driver differential 5-GHz clock output (−0.5% SSC-on) with 31.5-kHz modulation frequency.

Fig. 19 (a) is the block diagram of the jitter measurement system using an oscilloscope, while Fig. 19(b) indicates a real serial-link system. The clock recovery block of an oscilloscope, for jitter measurement, can be turned off as the constant frequency mode and turned on as the tracking mode. In the constant frequency mode, the reference frequency for jitter measurement is set as the input average frequency. On the contrary, in the tracking mode, the reference frequency in the oscilloscope is the recovered clock, which can mimic the RX of a real serial-link system with CDR and CTLE. The jitter measurement results for both modes are provided in Table II.

The time-domain specifications of the SSCG are measured using MSOV334A in the differential mode. Fig. 20 demonstrates the triangular output frequency, indicating that the modulation frequency is about 31.5 kHz with −0.5% modulation depth. As a clock source for SerDes/transceiver, it is more important to evaluate the jitter performance at the RX side. Therefore, rms jitter result with clock recovery is a key specification for our applications. The eye diagram is measured using the in-oscilloscope second-order clock recovery with 6-MHz observed jitter transfer function (OJTF) and 1.0 damping factor. Fig. 21 shows the measured eye diagram of the SST driver with disabled SSC. The peak-to-peak differential output voltage is about 600 mV. The random rms jitter RJ_{rms} and the deterministic jitter $DJ_{\delta\delta}$ are 630 and 570 fs, respectively. With −0.5% SSC-on, RJ_{rms} and $DJ_{\delta\delta}$ are both increased to 640 and 730 fs, respectively, as shown in Fig. 22, because of the frequency nodulation. Compared with the simulated RJ_{rms}, the measured jitter increases by 220 fs, which is mainly due to the power supply noise. The rms jitter difference between the simulation and measurement can also indicate that the 3-dB loss of EMI reduction comes from the extra noise, which reduces the PSD at the 5-GHz center frequency. To verify the reliability of the proposed SSCG, the jitter of the 5-GHz output is measured at different temperatures. Fig. 23 shows

TABLE II
PERFORMANCE SUMMARY AND COMPARISON OF THE SSCG

Specifications	TCAS-I'10 [10]	JSSC'11 [6]	ASSCC'15 [2]	ASSCC'17 [8]	TCAS-I'13 [4]	JSSC-15 [15]	JSSC-12 [17]	TCAS-I'13 [14]	**This work**
Technology (nm)	130	90	65	180	90	28	130	180	**55**
Fo (GHz)	3	6	3.2	1.5	6	3.3	3.5	1.5	**5**
Supply (V)	1.2	1	1	1.8	1.2	1	---	1.8	**1.2/2.5**
Modulation scheme	$\Delta\sum$ with chaotic	PI	$\Delta\sum$	DTC SSPLL	Self-oscillating	PI	$\Delta\sum$ with N-R mod.	All digital	**PI with linear mod.**
Modulation freq. (KHz)	33	32.95	30	32	31.5	30MHz@f_{clk}=500MHz	31	33	**31.5**
EMI reduction (dB) @100KHz RBW	14.5	16.12	11	16.37	12.5	27 @10%	19.14	14.37	**19.44** @ -0.5% D-S
$Jitter_{rms}$ (ps) (clock recovery off)	---	---	---	---	---	---	---	---	**14.9**
$Jitter_{rms}$ (ps) (ssc_off)	5.4	0.71	2.98	0.88	1.2	3.16	2.44	1.49	**0.63**
(ssc_on)	---	0.77	---	---	2	---	---	2.67	**0.64**
$Jitter_{p-p}$ (ps) (ssc_off)	---	7.79	---	---	---	---	16.15	13.33	**9.53**
(ssc_on)	---	8.54	---	---	15	---	---	19.9	**9.9**
Normalized power dissp. (mW/GHz)	4.9	4.6	1.98	7.4	2.4	8.88	6.78	15.6	**9.3**
Core area (mm^2)	0.27*0.78	0.55*0.45	0.271	0.467	0.533	0.031	0.076	0.301	**0.092**

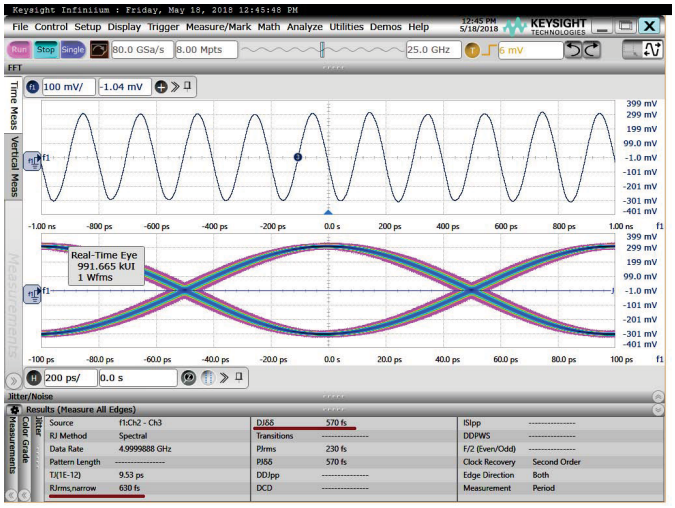

Fig. 21. Measured eye diagram of the SST driver differential 5-GHz clock output (SSC-off), $RJ_{rms} = 630$ fs and $DJ_{\delta\delta} = 570$ fs.

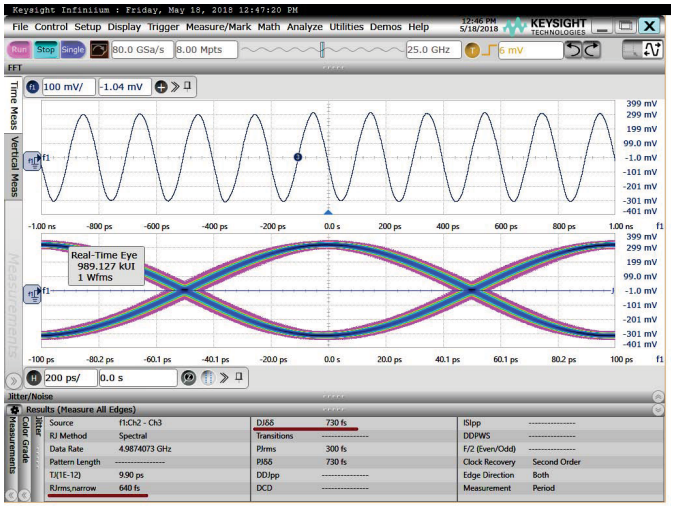

Fig. 22. Measured eye diagram of the SST driver differential 5-GHz clock output (-0.5% SSC-on), $RJ_{rms} = 640$ fs and $DJ_{\delta\delta} = 730$ fs.

the measurement results of total/deterministic/random jitters with case temperatures (Tc) from 27 °C to 125 °C. It shows that the random and deterministic jitters are not affected by temperature variations, whereas the total jitter increases from 9.5 to 10.4 ps.

Table II summarizes the performance of this article and compares them with previously reported SSCGs with multi-gigahertz output clock frequencies. The proposed SSCG achieves the state-of-the-art 19.44-dB EMI reduction and 640-fs rms jitter in 5-GHz operating frequency. All the results are summarized under 100-kHz RBW, and only the EMI reduction performance in [17] is comparable to this article, but with significantly larger rms jitter (2.44 ps). Theoretically, using Newton–Raphson MP as [17] can further improve the EMI reduction performance of the proposed design and is part of our future work. The power consumption distribution is reported in Fig. 24. The total power of the core is 46.54 mW, where about 78% is consumed by the VCO. The structure of the RO we used is similar to the design in [27]. Compared with other types of VCO, this inverter-based pseudodifferential two-stage RO is more area efficient and has acceptable phase noise for 10-Gb/s SerDes application. To oscillate as high as 5 GHz in this article, about 15-mA bias current is applied in the RO for the design specification of less than 0.7-ps rms jitter. The average current consumption can be reduced with transistor size scaled down by sacrificing the jitter performance. For higher output frequency SSCG design, such as 10 GHz, LC-VCO is more popular than RO, which can obtain a better tradeoff between power consumption and jitter, at the cost of more chip area. The power consumption is normalized

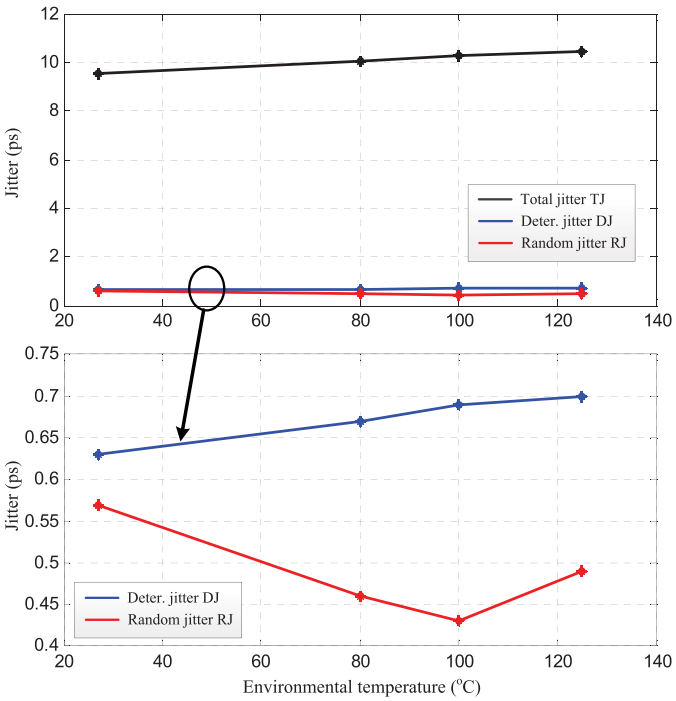

Fig. 23. Measured TJ, DJ, and RJ versus case temperatures Tc from 27 °C to 125 °C.

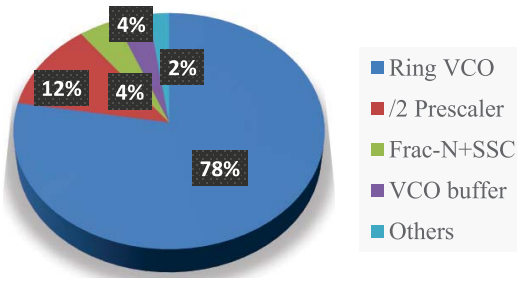

Fig. 24. Power consumption distribution of the proposed SSCG. The total power of the core is 46.54 mW.

as mW per GHz in Table II, and the proposed design shows a moderate-power efficiency characteristic, which should be optimized in the future works.

V. Conclusion

In this article, a charge-pump phase-compensated SSCG is proposed with the state-of-the-art 19.44-dB EMI reduction performance under 31.5-kHz modulation frequency and 0.5% down-spread. The SSCG uses traditional triangular MP associated with the proposed scaled resistor-based static logic PI. The 32-slice scheme is adopted to increase the phase interpolation resolution. The proposed design is fabricated using a 55-nm CMOS process with 0.092-mm^2 core area and 9.3-mW/GHz power efficiency under 5-GHz output clock frequency. The proposed chip can operate up to 125 °C case temperature with less than 10.4-ps total jitter. When SSC is turned on, the random rms jitter only increases 10 fs. The modulation frequency, depth, and frequency divisor can be programmed according to the applied protocols. The proposed SSCG has been applied to industrial 10-Gb/s SerDes links, such as JESD204B and SATA.

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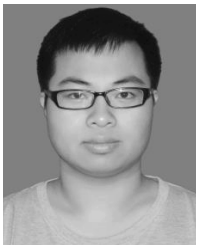

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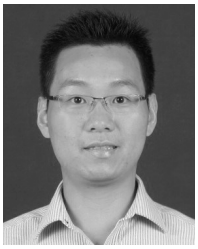

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