A 100-ppm Integrated TDM-Based Single-Phase Wattmeter for Smart Grid

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***Abstract*—In this brief, the Time-Division Multiplier (TDM)-based electronic wattmeter has be integrated for the first time. To integrate the wattmeter and properly select parameters for its circuit, this brief provides the modeling of TDM and the theoretical analysis of three types of errors, which improved the TDM theory. Based on these analysis, the considerations for designing the circuits of the modules of TDM are provided. Besides, the analysis using root locus theory for notch filter design are also provided, which simplified the initialization and determination of the design parameters. The wattmeter circuits, whose maximum input voltage and current amplitudes are ±15 V and ±2.5 mA respectively, is integrated into a chip manufactured by a 0.35-μm high-voltage semiconductor process and occupying area of 1.6 × 2.5 mm^2. And the precision of this integrated wattmeter is sub-100 ppm, represented by relative systematic error.**

***Index Terms*—Time-division multiplier, wattmeter, error analysis, notch filter.**

I. Introduction

With more and more renewable energy are connected to the grid, the whole grid system become more and more complicated [1]. As spreading and implementing of the idea of smart grid, the demanding for wattmeters, the eye of the grid system, are tremendous increasing, as well as for better performance. Traditional wattmeters implemented by discrete components suffers from high cost for massive deployment and upgrade. By taking the advantage of the semiconductor process, with relatively mature process, the cost can be greatly reduced.

The basic usage scenario of wattmeter is measuring electric energy. The diagram of a electric energy measurement system is shown in Fig. 1. Since the voltage and current from the gird is too large to process by common electronic components, scaling down is necessary and accomplished by transformer,

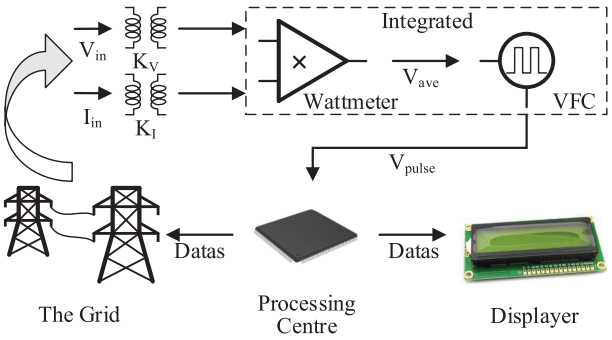

Fig. 1. The diagram of a electric energy measurement system.

K_V and K_I. The wattmeter is use to calculate the active power which is represented by voltage quantity at the output. But, to obtain value of electric energy, the integration of this voltage quantity is confined by supply voltage of the circuit. Therefore, the voltage quantity must be converted to other quantity, so the Voltage Frequency Converter(VFC) is introduced. The output of VFC is pulse wave that can be countered by digital processing unit. The calculated value is representing the electric energy that can be displayed on displayer or sent to power line carrier communication module to realize remote meter reading which is needed by smart grid. Generally, Wattmeter and VFC are implemented by analog circuits which are suitable for integration. In Fig. 1, the wattmeter is only used for single phase, but the three-phase grid measurement can realized by two or three single-phase wattmeters. Due to the feature of integration, the cost for integrated single-phase wattmeters are lowered again. But for discrete wattmeters, the cost on the components becomes higher.

In wattmeters, multiplication is the most significant operation, therefore the performance of multiplier is vital. Compare to the universal analog multiplier, Time-Division Multipliers (TDM) are more suitable for active power measurement in grid because the TDM has better linearity in lower frequency region. Even though the TDM are used in power measurement for nearly seventy years, but during this time, the implementation of TDM is always discrete and its basic theory stagnated for recent two decades [2], [3]. The outdated theory is unable to reveal the relationship between design parameters and performance of TDM, and this relationship is vital to integrated circuit design since the parameters in integrated circuit are hard to change. Here in this brief, this theory gap is filled. Moreover, when integrating the filter in TDM, this brief

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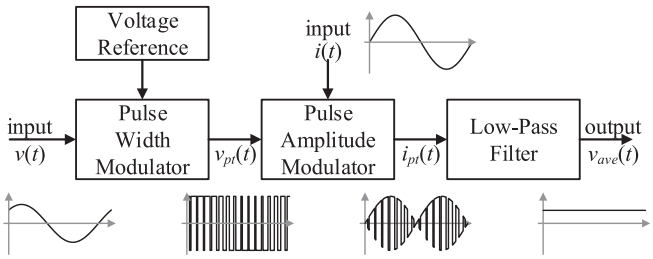

Fig. 2. The block diagram of a Time-Division Multiplier.

introduced the root locus to analyse the filter which simplified the design of multi-zeros and poles filter.

This brief is organized as follow: Section II is modeling and analysing the TDM; Section III gives wattmeter circuit and design consideration, and how root locus apply to notch filter design; Section IV shows the results of this integration; and Section V draws some conclusions.

II. Improvement of TDM Theory With Error Analysis

A. Basic Principle of TDM

In grid, where both voltage and current are both sinusoidal and the frequencies are the same, the power is the product of voltage and current of the energy signal and expressed as

$$\begin{aligned} p(t) &= v(t) \times i(t) \\ &= \frac{1}{2} V_m I_m \cos\phi - \frac{1}{2} V_m I_m \cos(2\omega_0 t + \phi), \end{aligned} \tag{1}$$

where ω_0 is the signal angular frequency, V_m and I_m are amplitude of input voltage and current, and ϕ is the phase difference between voltage and current, and $\cos\phi$ is called power factor. $p(t)$ is varying over time, and called instantaneous power. When calculating the electric energy a time that is integer multiple of signal period, the remains is first component of Eq. (1) and called average power or active power.

The block diagram of TDM is shown in Fig. 2 [4], where the waveform of marked signal is also shown. The input voltage, $v(t)$, is converted to a pulse train $v_{pt}(t)$ whose duty cycle is proportional to the value of input voltage. And then the input current, $i(t)$, modulates the amplitude of $v_{pt}(t)$ with its value. Finally, the new pulse train, $i_{pt}(t)$, is sent to the Low-Pass Filter (LPF) to obtain the DC component which is the corresponding active power. When the inputs are both DC signal, the value of output of filter is

$$V_{ave} = \frac{1}{k_I} VI. \tag{2}$$

But when the inputs are both sinusoidal signal, calculation of the value of V_{ave} requires a assumption that the frequency of $v_{pt}(t)$ is much higher than that of input signal. In this case, in a period of pulse, the input signal can be viewed as DC signal. Thus, DC component in this period can be calculated by Eq. (2). In this short time, the result is also regarded as instantaneous power of input signal. So the DC component of entire input signal period, T_0, is

$$V_{ave} = \frac{1}{T_0} \int_0^{T_0} \frac{1}{k_I} v(t) i(t) dt = \frac{1}{2k_I} V_m I_m \cos\phi. \tag{3}$$

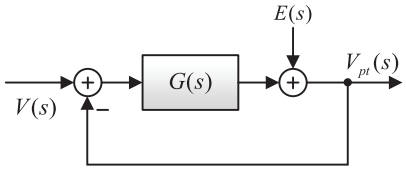

Fig. 3. The structure of Pulse Width Modulator of Goldberg type.

According to Eq. (1), the integration can be simply realized by filtering out the double frequency component. Because the frequency in grid is relatively low, in addition to traditional LPF, the notch filter is also required. But the design of notch filter is always neglected by TDM-design literatures because LC filters are easily implemented discretely [5], [6].

B. System Modeling of TDM

The structure of Pulse Width Modulator (PWM) of Goldberg type can be modeled as negative feedback structure consisted of integrator and quantizer, shown in Fig. 3, where $E(s)$ is the quantization noise that is introduced by 1-bit quantizer realized by comparator. So the s-domain expression of output of Modulator is

$$V_{pt}(s) = \frac{G(s)}{1+G(s)} V(s) + \frac{1}{1+G(s)} E(s), \tag{4}$$

where the functions that $V(s)$ and $E(s)$ multiplied is called Signal Transfer Function (STF) and Noise Transfer Function (NTF), respectively. They are introduced by characteristic of negative feedback. When $G(s) = 1/(s\tau)$ where τ is time constant of integrator, the STF is low-pass characteristic and the NTF is high-pass. Hence, for a sinusoidal input, the signal component of Eq. (4) in time domain is

$$v_{ptS}(t) = \frac{V_m}{\sqrt{1+(\omega_0\tau)^2}} \sin(\omega_0 t + \arctan\omega_0\tau), \tag{5}$$

where both the amplitude and phase of input voltage are changed by the low-pass characteristic of STF.

During pulse amplitude modulating, if considering pulse train amplitude modulating the input current rather than another way around, the pulse train can be abstracted as sequences of 1 and -1, and the output of Modulator can be expressed as

$$i_{pt}(t) = \frac{1}{k_V} v_{pt}(t) \times i(t). \tag{6}$$

By understanding the modulation in this way, the multiplication operation is directly realized. Because the input current is sinusoidal, the multiplication in time domain makes spectrum of $v_{pt}(t)$ shifted in frequency domain. If the changes due to STF is not eliminated, these changes would appear in $v_{ave}(t)$ causing error. To eliminate these changes, the input voltage can directly feed forward to output of $G(s)$ or the input of quantizer, and the output of Modulator is changed to

$$V_{pt}(s) = V(s) + \frac{1}{1+G(s)} E(s), \tag{7}$$

where the STF is 1 which is frequency free. This way of eliminating the changes is called phase compensation. Therefore, the TDM in Fig. 2 can be modeled as structure in Fig. 4.

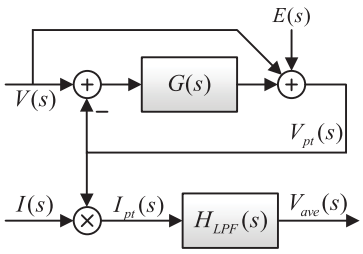

Fig. 4. The structure of modeled TDM.

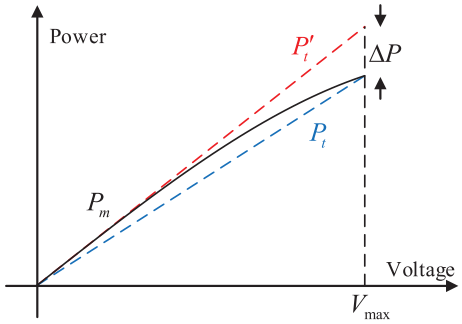

Fig. 5. Output characteristic of nonlinear TDM, when $a_3 < 0$.

C. Analysis of Errors in TDM

For an ideal measurement system, the output is perfectly linear to the input theoretically. But in reality, the systems are always nonlinear due to many reasons. The error between real and ideal system actually represents the precision of the system. So the precision of TDM-based wattmeters can be represented by relative error that is defined as maximum error between actual and theoretical over maximum result, which is

$$e = \frac{P_m - P_t}{P_{\max}}, \tag{8}$$

where P_m, P_t and $P_{\max}$ are measured power, theocratical power, and maximum power of the measurement system, respectively.

In PWM, if the phase compensation branch do not exist or compensated badly, according to Eq. (5) and (6), the DC component of output is contaminated by phase shift introduced by STF. And the error due to by phase shift, $\Delta\phi$, is

$$e(\phi) = -\tan\Delta\phi \sin\phi, \tag{9}$$

With power factor, $\cos\phi$, decreasing, the absolute value of relative error increases and reaches maximum value of $\tan\Delta\phi$ which is related to design parameter τ. And with the phase compensation, this error would be reduced to 0.

Because the wattmeter consists of other nonlinear modules, to determine the module nonlinearity according to system nonlinearity, the relationship of nonlinearity between system and modules must specific. For a slightly nonlinear system, its characteristic of input/output can be represented with Taylor expansion in the range of interest, which is

$$f(x) = a_1 x + a_2 x^2 + a_3 x^3 + , \ldots, \tag{10}$$

where $|a_2|, |a_3| \ll |a_1|$, and the coefficients of higher order in Eq. (10) are commonly less than a_2 and a_3 and often neglected. Taking Eq. (10) into account, if only the PWM is nonlinear, the value of output active power became to

$$V_{ave} = (a_1 + \frac{3a_3 V_m^2}{4}) \frac{V_m I_m \cos\phi}{2k_I}. \tag{11}$$

According to Eq. (11), the output characteristic of nonlinear TDM, when $a_3 < 0$, is depicted in black in Fig. 5. The red dot line is the theoretical output characteristic of linear TDM. Due to the error introduced by nonlinearity, its slope is unable to measure. So, the blue dot line representing the theoretical output characteristic of nonlinear TDM is responsible for calculating the relative error. In this case, the relative error of active power with input voltage amplitude of $xV_{\max}$ is

$$e(x) = 3HD_3 x(x^2 - 1), \tag{12}$$

where $x \in (0, 1]$, and HD_3 is representing third order harmonic distortion under maximum input voltage amplitude. The maximum error appeared at $x = \sqrt{1/3}$ and its value is proportional to HD_3. With the absolute value of HD_3 decreasing, the absolute value of error is also decreasing. Similar procedure would take place when analysing nonlinearity error of PAM for input current, and the result is also similar. But for modules behind the PAM, since the DC component is the wanted signal, according to Eq. (10), the error is

$$e(x) \approx \frac{a_2}{a_1} x^2 + \frac{a_3}{a_1} x^3 + , \ldots, \tag{13}$$

where nearly every coefficient of nonlinearity of modules is affecting the error.

Even though decreasing the input maximum voltage, or power in another word, decreases error introduced by nonlinearity, but the maximum cannot be too small. According to Eq. (7), the output of PWM contains the quantization noise. Due to frequency shift of the multiplication, the power of quantization noise at ω_0 shifted to DC and causing error. Unlike the two types of errors mentioned above that are fixed when the structures or circuits of modules are determined, the quantization noise error contaminate all power measurement results and varies over time. Even though the value of quantization noise error is unknown, according to Eq. (4), the quantization noise in lower frequency region is high pass filtered by NTF, which means it is controllable. So, using Eq. (8), the error of TDM when only considering the quantization noise is

$$e(x) = \frac{(\delta_x - \delta_0) - x(\delta_1 - \delta_0)}{a_1 P + \delta_1 - \delta_0}, \tag{14}$$

where

$$P_{\max} = 1/2 \cdot V_{\max} I_{\max},$$

and δ_0, δ_1 and δ_x are both produced by spectral shifting of quantization noise when the input power to maximum power ratio are 0, 1 and x, respectively. And they all follows

$$|\delta| = \left| \mathcal{F}^{-1}\{[NTF(j\omega)E(j\omega)]|_{\omega=\omega_0}\} \right|.$$

So decreasing the τ in NTF can possibly increases the performance of TDM.

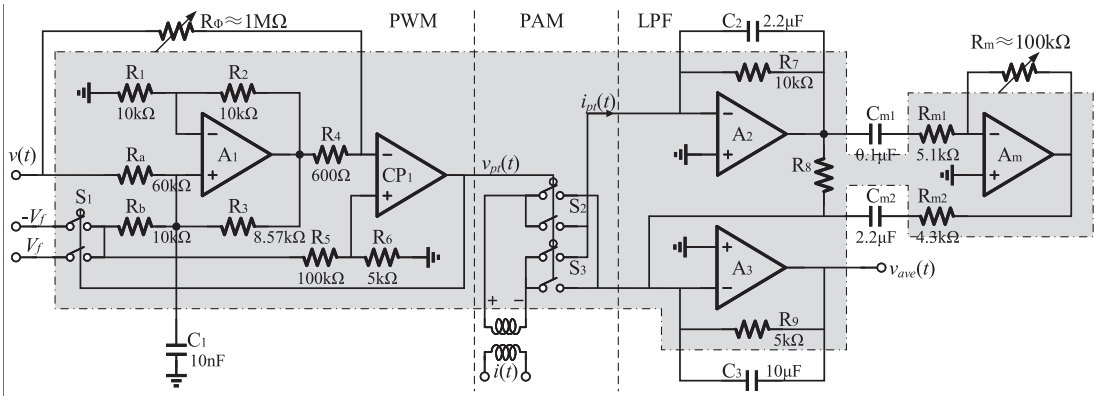

Fig. 6. The circuit schematic of Time-Division Multiplier.

III. Circuits Implementation of Integrated TDM

The circuit diagram of core portion of Time-Division Multiplier is shown in Fig. 6, where A_x, CP_x and S_x are representing the amplifiers, comparators and Single Pole Double Throw(SPDT) switch, respectively. The components in the gray region are all integrated. Because the working frequency of grid is relatively low, the capacitors in the circuit are too large to integrate.

To properly compensate the phase shift of PWM, the feed forward coefficient for PWM in Fig. 6 is

$$\frac{R_4}{R_\Phi} = a\frac{\cos\omega_0 t_0}{cb'/(\omega_0\tau) - \sin\omega_0 t_0} \tag{15}$$

where $a = 1/R_a$, $b' = R_\Phi/(R_\Phi + R_4)$, $c = (1 + R_5/R_6)$ and t_0 is the delay of the comparator, CP_1. And τ is also depending the power of quantization noise in PWM and equals to $R_aC_1R_5/R_6$. The nonlinearity error of PWM is depending on linearity of the amplifier under negative feedback, so increasing the DC gain of amplifier is very helpful. To cope with large current and capacitors, the type of amplifier is designed as Class-AB.

PAM is realized by two SPDT switches that can change the connection state of the input current source, hence the sign of $i_{pt}(t)$ is changing with the value of $v_{pt}(t)$, which realizing multiplication operation. The error of PAM is caused by the nonlinearity of on resistance of the switch. Decreasing the value of on resistance would decrease the nonlinearity.

The LPF circuit is consisted of two filters, notch filter and traditional LPF. The former is constructed by A_2, A_m and their circumjacent resistors and capacitors, and latter is constructed by A_3, R_9 and C_3. By using kirchhoff's current law on neg-input node of A_3, the simplified transfer function of the notch filters is

$$H_{nf}(s) = \frac{(1 + A + s\tau_1)(1 + s\tau_{m1})(1 + s\tau_{m2}) - ABs^2\tau_{m1}\tau_{m2}}{(1 + s\tau_1)(1 + s\tau_{m1})(1 + s\tau_{m2})}, \tag{16}$$

where

$$\tau_1 = R_7C_2,\ \tau_{m1} = R_{m1}C_{m1},\ \tau_{m2} = R_{m2}C_{m2},$$
$$A = R_7/R_8,\ B = (R_8R_m)/(R_{m1}R_{m2}).$$

Eq. (16) is a form that the root locus can apply to. According to root locus theory, the original zeros represented by the first portion of numerator is moving towards to final zeros represented by the second portion with a coefficient increasing from 0 to infinity. In second portion of numerator, R_m is the only parameter that does not change the original zeros, hence R_m is the variable coefficient of root locus. Since the final zeros are located in original point, two of the three zeros located at negative real axis should move towards to original point and one should move to infinity. Therefore, the shape of the root locus is determined and shown in Fig. 7. The intersection of zeros locus and imaginary axis is the location where the notch frequency should be. In this design, notch frequency is $2\omega_0$. For working frequency of 50 Hz, the design value is shown in Fig. 6.

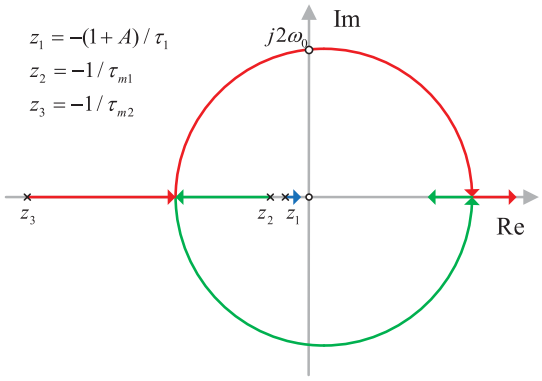

Fig. 7. The zeros locus of LPF.

IV. Simulation and Experimental Result

To obtain better linearity, the amplifier has DC gain of 129 dB and gain-bandwidth product of 46.1 MHz, the comparator has open-loop gain of 89 dB and delay of 270 ns with three SPDTs as load, and on resistance of switches in SPDT are all lower than 20 Ω in simulation. To confine the power of quantization noise, the balance frequency representing τ of PWM is set as 100 kHz. Because of larger input voltage would result in relatively poor linearity, the input scale resistor is set as 60 kΩ that leads to duty cycle of $v_{pt}(t)$ is around 30% to 70%. And the corresponding design parameters are shown in Fig. 6.

The integrated TDM-based wattmeter chip is manufactured by a 0.35-μm BCD high-voltage process, and the chip microphotograph is shown in Fig. 8. In order to satisfy the

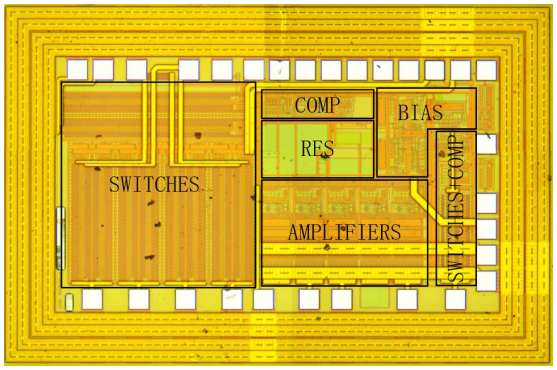

Fig. 8. Chip microphotograph of the integrated TDM-based wattmeter circuit.

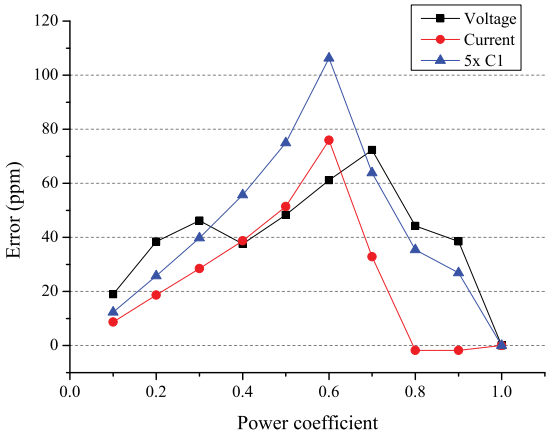

Fig. 9. Systematic error of this brief with different input power.

source voltage of ±15 V, asymmetric high-voltage MOSFETs are adopted, which greatly increased the area to 1.6×2.5 mm^2. In addition, the SPDT switches occupied about half of the area due to this high-voltage process. The power consumption of this chip is 2×15×0.0528 W, and about half of the power is used for exchanging the direction of input current.

The maximum amplitude of input voltage and current of this design are ±15 V and ±2.5 mA respectively. By setting the phase difference between input voltage and current to be 90 degree and adjusting the R_m, when the output become to 0, the phase error is well compensated. By changing the input amplitude of input voltage or current, the error over input power is measured. Between two available dies, well performed results are depicted in Fig. 9, where black and red lines belong to one die and representing the amplitude change of input voltage and current while the blue line belongs to another die and representing the error that the capacitance of C_1 in Fig. 6 increased 5 times with voltage amplitude change. As predicted, the maximum error appeared at around 60% of input power and larger quantization noise results in poor error performance, which proves that the frequency domain analysis of errors is correct.

According to Fig. 9, the error of chip is sub-100 ppm. Table I shows that the comparison between this brief to some previous works. Besides this brief, others implemented the wattmeter system discretely. Even though some works have better error performances than this brief, these better error performances rely on the high-performance components like ADCs which cost very much. Besides, based on analysis of error of this brief, migration between processes is easier, and better process may result in better error performance but massive-deployment cost will still be lower than discrete.

TABLE I
COMPARISON WITH SOME PREVIOUS WORKS

	[3] TIM 2017	[7] IMTC 2008	[8] IMTCP 2010	[9] CPEM 2016	**This work**
Method	TDM-based	Digital	PC-based	Digital	**TDM-based**
Implementation	Discrete	Discrete	Instrumental	Discrete	**CMOS 0.35μm process**
Voltage range (V)	0~±240	N/A	1~16 -1~-16	0.8~±230	**0~±15***
Current range (A)	0~±5	0~±1	1~10 -1~-10	0~±5	**0~±2.5m***
ADC resolution(bits)	22	18	24	N/A	**N/A**
Error (ppm)	50	200	60	30	**100**

* Input voltage and current ranges of this work is scaled by transformers.

V. CONCLUSION

A TDM-based wattmeter for the Grid is integrated for the first time. With frequency domain analysis, three main errors in TDM are revealed, and they are phase shift error, nonlinearity error and quantization noise error. By adding phase compensation branch, limiting input maximum voltage and increasing balance frequency of PWM, these error could be eliminated or decreased and result in better linearity of measurement system. Finally, for designing multi-zero filter, root locus theory can tremendously simplify the parameter design procedure.

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