A Chopper Instrumentation Amplifier with Amplifier Slicing Technique for Offset Reduction

Tsz Ngai Lin, Bo Wang, Samir Brahim Belhaouari and Amine Bermak
Division of Information and Computing Technology, College of Science and Engineering,
Hamad Bin Khalifa University, Doha, Qatar

***Abstract*—This paper presents a chopper instrumentation amplifier design that employs a proposed amplifier slicing technique for offset reduction. In this scheme, the core amplifier is split into multiple identical slices. During operation, the offset polarity of these slices is firstly determined by employing the second-stage of the amplifier as a static comparator. Next, by using the polarity information, the amplifier slices are regrouped to achieve statistical offset suppression. A mathematical model is developed in this paper to estimate the effectiveness of this reduction scheme. The sliced amplifier structure also enables a scalable noise and bandwidth without adding extra analog components. Simulation results show that the proposed reduction scheme achieves a $>$ 40 dB offset suppression and a noise efficiency factor (NEF) of 2.2. The circuit is implemented in a 0.18 μm standard CMOS technology for proof of concept and consumes 0.4 μA to 1 μA current from a 1.2 V supply to reach a noise level from 90 nV/$\sqrt{}$Hz to 31.8 nV/$\sqrt{}$Hz, respectively.**

I. Introduction

Sensor readout circuits require a low noise instrumentation amplifier (IA) and a high-resolution analog-to-digital converter (ADC) to preserve the signal for the next stage [1]. Up to now, various instrumentation amplifier structures have been introduced to fulfill the needs of amplifying small differential signals while rejecting large interference. Particularly, capacitively-coupled IA (CCIA) that makes use of the capacitive-gain network is gaining popularity because it avoids transconductance stages in the feedback path and therefore exhibits higher energy-efficiency [1], [2], [3], comparing to its counterparts such as current-feedback IA (CFIA) or 3-amp IA topology [4]. However, like all the other amplifiers, the input-referred offset (at mV-level in modern CMOS technologies) still bothers the CCIA design [5].

Different techniques are developed to reduce the offset in CCIA. For example, replacing devices with larger dimensions and drawing layout with good matching. Dynamic offset cancellation techniques like auto-zeroing and chopping can also be applied to suppress the effective input-referred offset to μV-level [6]. However, auto-zeroing requires a sample phase and is difficult (or costly) to be applied in continuous signal applications. The chopping technique, on the other hand, alternates the polarity of the input signal and modulates the offset to a higher frequency, needs additional filtering [4].

Because of the implementation simplicity, the effectiveness of suppressing offset and low-frequency noise, and the merits of maintaining continuous output, the chopping technique is frequently used in CCIA designs. However, as mentioned above, the modulated offset induces a large ripple in the output

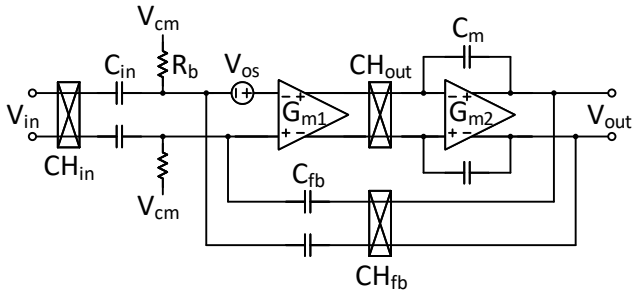

Fig. 1. Structure of a standard CCIA.

on top of the actual amplified signal, which greatly limits the amplifier's output range and must be suppressed. Several ripple-reduction loops are proposed to minimize the undesired ripple, like through a current-feedback [2] or voltage-feedback stabilizing loop [7]. Filtering is another way to produce a ripple-free output [3], [8]. However, both the feedback and filtering schemes require extra components which become drawbacks when area and power are the main concerns of sensor readout circuits [3].

In this paper, a CCIA offset reduction scheme using a dynamic amplifier slicing technique is proposed [9], [10]. Specifically, for CCIA using a two-stage amplifier, the offset polarity of the first-stage amplifier can be detected by shorting its inputs and employing the second-stage amplifier as a comparator. By dividing the first-stage amplifier into multiple slices, the offset polarity of each slice can then be determined. Using such information, these slices can be dynamically grouped to form the final amplifier with offset minimization. The reduction scheme only need to perform once before each operation. If memory is available, the slicing configuration can be stored on-chip as well. Since there is no extra analog component added to the circuit, power can be conserved. Benefiting from the amplifier slicing technique, there is a degree of freedom to tune the noise and bandwidth of the amplifier as well, which makes the amplifier more universal for sensor readout circuits [11].

This paper is organized as follows. Section II introduces the structure of standard CCIA. Section III explains the amplifier slicing technique. This section also includes the proposed offset reduction scheme and the developed mathematical model. The extra benefits of this offset reduction scheme, namely, scalable amplifier noise and bandwidth, are also discussed.

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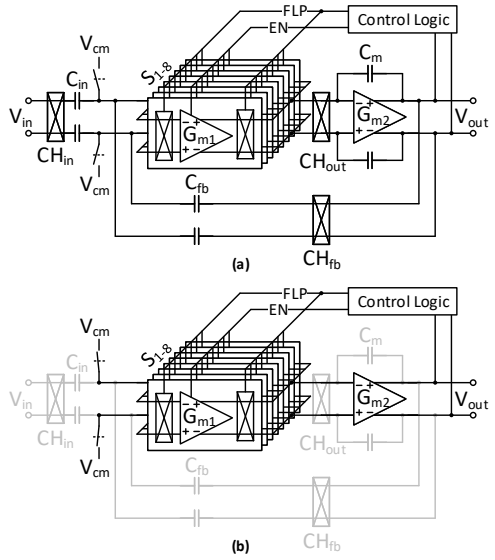

Fig. 2. (a) Proposed CCIA with offset reduction scheme using amplifier slicing technique (b) Offset reduction scheme in operation.

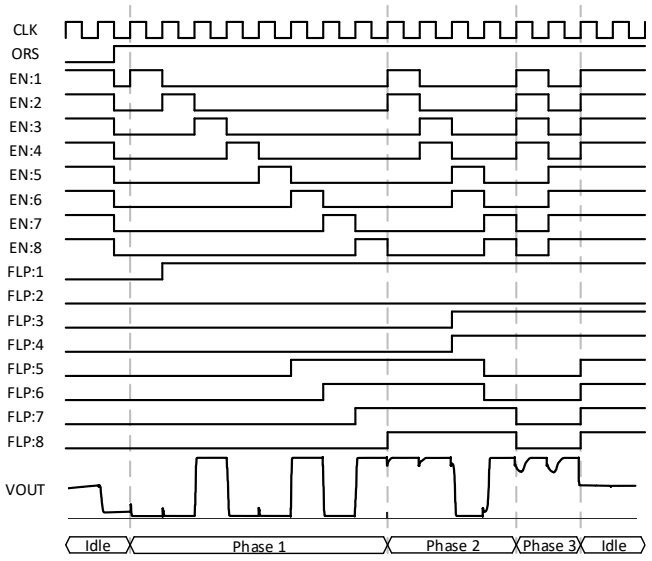

Fig. 3. Timing diagram of the offset reduction scheme.

Section IV includes the circuit implementation and simulation result of a proof-of-concept design in a 0.18 μm standard CMOS process. Section V concludes this paper.

II. Capacitively-coupled Chopper Instrumentation Amplifier

The structure of a standard CCIA is shown in Fig. 1. The core is a two-stage amplifier (G_{m1} and G_{m2}) with a capacitive-gain network (C_{in}/C_{fb}) . By inserting choppers (CH) in the signal path, signals are modulated between low frequency and chopping frequency (f_{chop}). Low-frequency input signal is chopped to high frequency by input chopper (CH_{in}) before amplification. Output chopper (CH_{out}) de-chops the high-frequency signal back to DC while modulates the amplifier offset (V_{os}) to high frequency. After integrating on C_m through second stage, the de-chopped input signal appears at the output and the offset in high-frequency accompanies as a ripple.

Since an offset current $I_{offset} = V_{os} \times G_{m1}$ is charging or discharging C_m within half chopping cycle $1/2f_{chop}$, the ripple voltage can be estimated as follows:

$$V_{ripple} = I_{offset} \times \frac{1/2f_{chop}}{C_m} = \frac{V_{os} \times G_{m1}}{2 \times f_{chop} \times C_m} \qquad (1)$$

where V_{os} and G_{m1} are the inherent offset and transconductance of the first stage, f_{chop} is the chopping frequency and C_m is the miller compensation capacitor. Inherent amplifier offset is hard to eliminate as device mismatch always appear in manufacturing. Thus, ripple always appears and must be suppressed to prevent output saturation. In practise, G_{m1} is restricted by the system noise requirement. Many designs prefer using a higher chopping frequency and a larger miller compensation capacitor to obtain a smaller ripple voltage. However, high chopping frequency leads to a larger input bias current and a potential gain drop while large capacitor increases the chip area significantly [12].

III. Amplifier Slicing Technique

The proposed CCIA with the offset reduction scheme is shown in Fig. 2(a). In this design, the first stage amplifier is divided into eight identical slices $S_{1\text{-}8}$. Slices are controlled by a pair of flipping switches and enabling switches. Every flipping switch is connected to its control signal (FLP) to flip its polarity. Every enabling switch is connected to its control signal (EN) to enable or disable the slice. The width of transistors in each amplifier slice shares one-eighth of the original amplifier size. Thus, the transconductance is also one-eighth of the original while the output impedance is eight times larger, which keeps the intrinsic gain unchanged.

A. Offset Reduction Scheme

During offset reduction, as shown in Fig. 2(b), the capacitive feedback loop is broken, the miller compensation capacitors are disconnected and inputs of the first stage are shorted. The second stage G_{m2} acts as a comparator. The timing diagram of the offset reduction scheme is shown in Fig. 3.

During the first phase, the control logic enables the amplifier slices one by one and takes the comparator outputs correspondingly. Since inputs are shorted, the offset is amplified by the intrinsic gain of $S_{1\text{-}8}$ and passed to G_{m2}. The input-referred offset of G_{m2} is suppressed by the intrinsic gain of G_{m1}. Thus, comparing to the amplified G_{m1} offset, the inherent offset of G_{m2} can be omitted. Therefore, G_{m2} only outputs the polarities of the amplifier slices offset. For odd slices, the control logic flips the slices if the offset is positive. For even slices, the control logic flips the slices if the offset is negative. If any amplifier is flipped, the polarity of its offset is reversed. Thus, the polarities of neighboring slices are always opposite.

During the second phase, the control logic enables the amplifier slices two by two and takes the comparator outputs correspondingly. For every two slices, since the offset polarities are opposite after the first phase, the resulting offset is

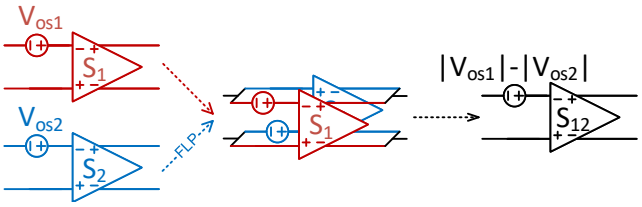

Fig. 4. Resulting input-referred offset after combining two slices.

smaller after combining two slices. Assuming the offset of slices S_1 and S_2 are V_{os1} and V_{os2}. The offset of the combined slices S_{12} is $V'_{os1} = |V_{os1}| - |V_{os2}|$, as shown in Fig. 4. Again, the control logic decides to flip the combined amplifier slices $S_{12}, S_{34}, S_{56}, S_{78}$ to make sure the polarities are opposite.

During the last phase, the control logic enables the amplifier slices four by four and takes the comparator outputs correspondingly. Assuming the offset of combined slices S_{12} and S_{34} are V'_{os1} and V'_{os2}. The offset of the combined slices S_{1234} is $V''_{os1} = |V'_{os1}| - |V'_{os2}|$. Once again, the control logic decides to flip the combined amplifier slices S_{1234} and S_{5678} to make sure the polarities are opposite. The offset reduction is done and all slices $S_{1\text{-}8}$ are enabled for normal operation.

A total number of $2\times(2^n\text{-}1)$ polarity comparisons are needed for 2^n slices. Comparing to the differential-pair matching scheme [9], which needs 924 cycles to brute force all combinations for the smallest offset of 6 differential-pair, the number of comparison cycles are much less. In addition, the differential-pair matching scheme requires a closed-loop configuration to sample every offset and search for the smallest one. This offset reduction scheme is carried out under open-loop configuration to dramatically reduce the settling time.

B. Mathematical Model

The concept of the offset reduction scheme is to make sure the offset polarities of slices are always opposite such that after combining the slices, the offset amplitude is always reduced. A mathematical model is derived to show the reduction of offset deviation. In this model, the calculation is based on splitting the amplifier into eight identical slices (n = 3). The number of slices can be further increased by reducing the width of the transistor size in every slice. However, more enabling and flipping switches are needed while the variance reduction is less significant.

Assuming the original offset (V_{os}) of an amplifier follows a Gaussian distribution with zero mean and a variance of σ^2, which can be expressed as:

$$V_{os} \sim \mathcal{N}(0,\, \sigma^2)\,. \tag{2}$$

The offsets of amplifier slices $S_{1\text{-}8}$ ($V_{os1\text{-}8}$) follow a Gaussian distribution with zero mean and variance $\sigma^2/8$, which can be expressed as:

$$V_{os1\text{-}8} \sim \mathcal{N}(0,\, \frac{\sigma^2}{8})\,. \tag{3}$$

If there is no offset suppression, since all amplifier slices $S_{1\text{-}8}$ are independent, the resulting offset follows the same distribution as the original offset:

$$V_{os1} + V_{os2} + ... + V_{os8} = V_{os} \sim \mathcal{N}(0,\, \sigma^2)\,. \tag{4}$$

However, during the offset reduction scheme, only the magnitude is considered. Therefore, the absolute value of $S_{1\text{-}8}$ offsets ($|V_{os1\text{-}8}|$) follow a half-normal distribution instead [13], which can be expressed as:

$$|V_{os1\text{-}8}| \sim \mathcal{H}(0, \frac{\sigma^2}{8}(1-\frac{2}{\pi}))\,. \tag{5}$$

After combining two amplifier slices (n = 1), the resulting offsets $V'_{os1\text{-}4}$ still follow half-normal distribution, which can be written in the following notation, where $i = 1, 2, 3, 4$

$$V'_{os1\text{-}4} = |V_{os2i\text{-}1}| - |V_{os2i}| \sim \mathcal{H}(0,\, \frac{\sigma^2}{4}(1-\frac{2}{\pi}))\,. \tag{6}$$

After combining four amplifier slices (n = 2), the resulting offsets $V'_{os1\text{-}2}$ are the difference of the absolute value of $V'_{os1\text{-}4}$, the distribution is changed and can be estimated as:

$$V''_{os1\text{-}2} = |V'_{os2i\text{-}1}| - |V'_{os2i}| \sim \mathcal{U}(0,\, \frac{\sigma^2}{2}(1-\frac{2}{\pi})^2 \times 2^{0.116})\,, \tag{7}$$

where $n^{0.116}$ is the error correction function for offset variance of 2^n slices. After combining all eight amplifier slices together (n = 3), the resulting offset V'''_{os} is the difference of the absolute value of of $V''_{os1\text{-}2}$, the distribution is changed again and can be estimated as:

$$V'''_{os} = |V''_{os1}| - |V''_{os2}| \sim \mathcal{W}(0,\, \sigma^2(1-\frac{2}{\pi})^3 \times 3^{0.116})\,. \tag{8}$$

The mathematical model of the offset reduction scheme is built and run multiple times to verify the change in distribution and variance reduction. As shown in Fig. 5, the offset distribution of a different number of slicing is plotted. Comparing the amplifier original offset (V_{os}) to the resulting offset with two slices ($V'_{os1\text{-}4}$), the distribution changes from normal distribution to half-normal distribution and the variance is smaller. When the number of slices is increased to four ($V''_{os1\text{-}2}$) and eight (V'''_{os}), the variance is getting less sparse but the reduction is less significant. Nevertheless, for 2^n slices, the offset variance is $\sigma^2(1-\frac{2}{\pi})^n \times n^{0.116}$.

C. Dynamic Noise and Bandwidth

Reconfigurable readout circuits are commonly used in sensor signal conditioning because the signal property of different sources varies a lot. Features such as programmable gain [1] or scalable noise [14] are being added to the circuits. Likewise, the amplifier slicing technique gives a degree of freedom for any individual amplifier slice to operate separately and achieves a scalable noise.

Since each amplifier slice shares a portion of the original amplifier, the equivalent transconductance can be varied by enabling/disabling some amplifier slices. Whenever a higher noise level can be tolerated, some amplifier slices can be disabled. The power consumption, on the other hand, can be reduced because those disabled slices consume little current.

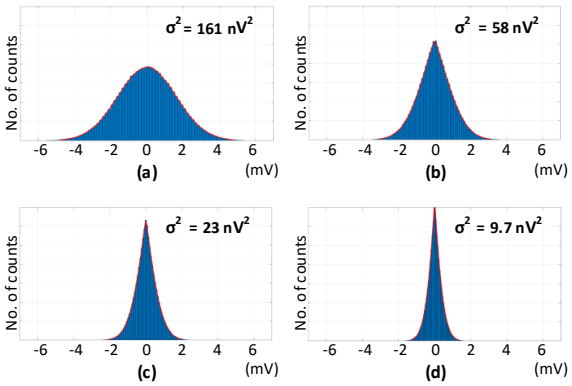

Fig. 5. Offset distribution with offset reduction scheme after (a) no slicing, (b) 2 slicing, (c) 4 slicing, (d) 8 slicing.

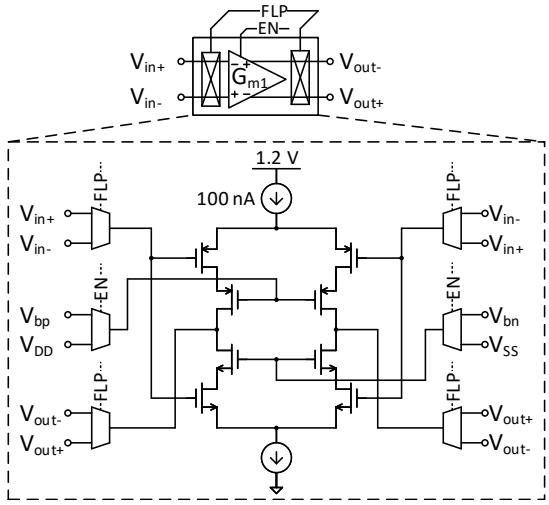

Fig. 6. Simplified schematic of one amplifier slice with switches.

The unity-gain bandwidth (GBW) of the amplifier changes if the equivalent transconductance is altered, which is undesired in some applications. However, if the input and feedback capacitor C_{in} and C_{fb} are sliced together with the amplifier, the GBW remains unchanged as the ratio is fixed between transconductance and capacitance. Nonetheless, there is always a trade-off between power and offset when disabling amplifier slices because the offset deviation is expected to increase as there are fewer slices for the scheme to reduce offset.

IV. Circuit Implementation and Simulation Result

The proposed amplifier with the slicing technique is realized in a 0.18 μm standard CMOS technology with a 1.2 V supply. As shown in Fig. 6, the first stage is a combination of eight identical cascoded inverter-based amplifiers with enabling and flipping switches. With one-eighth of the input-pair sizing ($\frac{240\mu m}{10\mu m} \times \frac{1}{8}$), the transconductance G_{m} and the intrinsic gain is 2.5 μS and 80 dB per slice, respectively. Each slice consumes 100 nA when enabled. The second stage is a standard common-source amplifier and the biasing current is chosen to

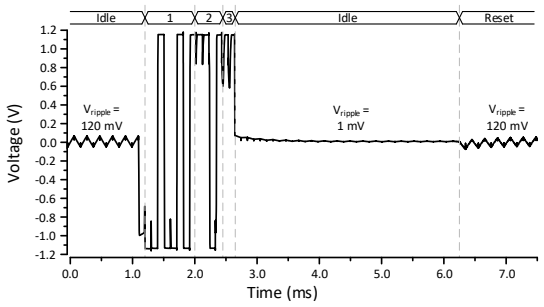

Fig. 7. Transient simulation showing suppressed offset induced ripple.

TABLE I
Performance Summary

	This work	[2]	[8]	[9]
Technology	0.18μm	65nm	0.6μm	0.18μm
Offset voltage (μV)	25	1	3	3.5
Chopping frequency (kHz)	5	5	125	500
Input noise (nV/$\sqrt{\text{Hz}}$)	90 - 31.8	60	55	13.5
NEF	2.2	3.3	8.7	7.2
GBW (kHz)	25.4 - 203	70	350	32000
Supply current (μA)	0.4 - 1	1.8	17	194
Supply voltage (V)	1.2	1	1.8 - 5.5	1.5

be 200 nA. The miller compensation capacitor is 50 pF and the chopping frequency is 5 kHz. The input and feedback capacitor C_{in} and C_{fb} are designed to be 20 pF and 0.2 pF, respectively. In close-loop configuration, the amplifier gain is fixed at 100 and the expected ripple voltage is $\frac{V_{\text{offset}} \times 20\mu S}{2 \times 5\text{kHz} \times 50pF} = V_{\text{offset}} \times 40$.

As the amplifier is split into 8 slices (n = 3), a total number of 14 comparisons are needed, which is 1.4 ms with a 10 kHz driving clock. The transient simulation is shown in Fig. 7. Before the offset reduction scheme started, the output suffers from a 120 mV ripple, which is equivalent to a 3 mV input-referred offset. After the scheme, the ripple is suppressed to 1 mV, achieving a $>$ 40 dB suppression. The large ripple reappears if the system is reset again.

Monte Carlo simulation is carried out to analyze the adopted CMOS technology. The variance of the input-referred offset (σ^2) is expected to be 172 nV^2. According to Eq. (8), the offset variance is reduced to $\sigma^2(1 - \frac{2}{\pi})^3 \times 3^{0.116} \approx 9.37$ nV^2. By disabling some slices, a scalable amplifier noise can be achieved as well. Table I summarized the amplifier performance with different slicing configuration and comparison to state-of-the-art IAs. By splitting the amplifier into eight slices, the offset voltage is reduced to 25 μV by Eq. (1). By reducing the input-referred offset from mV-level to μV-level, the offset reduction scheme suggested in this paper makes this amplifier suitable for CCIA application. Without increasing the circuit complexity or adding extra analog components, this work achieves excellent noise efficiency factor (NEF) [15] with low power consumption and decent offset reduction.

V. Conclusion

In this paper, an offset reduction scheme is proposed. Using the amplifier slicing technique, the amplifier can be split into smaller slices for offset comparison. By changing the offset polarity, the reduction scheme successfully reduces the offset to μV level with more than 40 dB offset suppression. Monte Carlo simulation shows the offset variation reduced from 172 nV^2 to 9.37 nV^2. The proposed CCIA also achieves good noise and power efficiency with 2.2 NEF implementing in a 0.18 μm standard CMOS technology. Dynamic noise and bandwidth are achieved from the reconfigurable structure. Operating from a 1.2 V supply, the circuit draws 0.4 μA to 1 μA current to obtain a noise range from 90 nV/$\sqrt{}$Hz to 31.8 nV/$\sqrt{}$Hz, respectively.

Acknowledgment

This publication was made possible by NPRP grant NPRP11S-0104-180192 from the Qatar National Research Fund (a member of Qatar Foundation). The statements made herein are solely the responsibility of the authors.

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